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High mobility graphene field effect transistors on flexible EVA/PET foils

Munis Khan[1,*], Jie Ji[2], Binbin Zhou[3], Peter U Jepsen[3], Peter Boggild[2] and August Yurgens[1]

[1] Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg 412 96, Sweden
[2] Department of Physics, Technical University of Denmark, Kongens Lyngby DK-2800, Denmark
[3] Department of Electrical and Photonics Engineering, Technical University of Denmark, Kongens Lyngby DK-2800, Denmark
[*] Author to whom any correspondence should be addressed.

E-mail: munis@chalmers.se

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Abstract

Monolayer graphene is a promising material for a wide range of applications, including sensors, optoelectronics, antennas, EMR shielding, flexible electronics, and conducting electrodes. Chemical vapor deposition (CVD) of carbon atoms on a metal catalyst is the most scalable and cost-efficient method for synthesizing high-quality, large-area monolayer graphene. The usual method of transferring the CVD graphene from the catalyst to a target substrate involves a polymer carrier which is dissolved after the transfer process is completed. Due to often unavoidable damage to graphene, as well as contamination and residues, carrier mobilities are typically 1000–3000 $cm^2\,(Vs)^{-1}$, unless complex and elaborate measures are taken. Here, we report on a simple scalable fabrication method for flexible graphene field-effect transistors that eliminates the polymer interim carrier, by laminating the graphene directly onto office lamination foils, removing the catalyst, and depositing Parylene N as a gate dielectric and encapsulation layer. The fabricated transistors show field- and Hall-effect mobilities of 7000–10 000 $cm^2\,(Vs)^{-1}$ with a residual charge-carrier density of 2×10^{11} 1 cm^{-2} at room temperature. We further validate the material quality by terahertz time-domain spectroscopy and observation of the quantum Hall effect at low temperatures in a moderate magnetic field of ∼5 T. The Parylene encapsulation provides long-term stability and protection against additional lithography steps, enabling vertical device integration in multilayer electronics on a flexible platform.

1. Introduction

Large, continuous, monolayer graphene is the most mature 2D material technology with many established and emerging applications and several large commercial providers. The applications span a wide range, including biosensors [1–6], high-frequency transistors [7], Hall sensors [8], high-speed electronics [9], conducting electrodes [10], flat lenses [11], and have been extensively covered in various recent reviews [12, 13]. The most common approach for large-area graphene by far is chemical vapor deposition (CVD) on copper foils [14–18] due to relatively simple synthesis process. As of today, the quality of the synthesized graphene, in terms of defect density and grain size, is no longer a bottle-neck. Remaining challenges for large-scale graphene production include: (i) the transfer of the graphene from catalytic copper to the target substrate [19, 20], often plagued with contamination, damage, wrinkles, as well as issues stemming from removal of the copper substrate [21], and (ii) the need for encapsulation, which is essential to provide chemical protection against contamination and mechanical protection to preserve carrier mobility and maintain consistency in electrical and optical performance. Numerous large-scale graphene transfer processes have been documented in the literature to address these challenges [22–24]. These processes encompass a wide range of techniques, including roll-to-roll methods [25–30], delamination transfer [31], transfer using various carrier polymers [19, 20], laser-assisted transfer [32], electrochemical methods [29], frame-assisted techniques [33], and semi-dry

transfer [34]. Previously, flexible GFET's on PET were reported using a self-healing gate dielectric [35]. The fabrication process involved a wet transfer of CVD graphene from copper to PET, with the charge-carrier mobility of merely 300 $cm_2\,(Vs)^{-1}$. Recently, Hong *et al* demonstrated a GFET made from roll-to-roll transferred CVD graphene on EVA/PET using the electrolytic gating, yielding field-effect mobility of 205 $cm_2\,(V\,s)^{-1}$ [31]. To the best of our knowledge, very few, if any, of these methods combine simplicity, consistently high carrier mobility, mechanical flexibility, and long-term protective encapsulation. This scarcity of a comprehensive solution may explain why, to date, no single transfer method has succeeded in establishing itself as a standard, akin to the CVD-synthesis on copper. The cleanest graphene device interfaces have been achieved in van-der-Waals heterostructures, particularly in graphene sandwiched between h-BN single-crystal flakes using dry transfer techniques [36–39]. Evidently, this technique is not scalable and relies on the availability and quality of other 2D materials.

Here, we present a simple transfer method that does exactly this. We report on a scalable and cost-effective process for fabricating top- and back-gated GFETs by using Parylene N as a dielectric layer for a wafer-scale CVD-grown graphene and lamination onto EVA/PET foils. CVD graphene on copper is coated with Parylene N dielectric using a process similar to that described in [30]. This method avoids the direct contact of the graphene with other polymers. These devices show a significantly reduced residual charge-carrier density, combined with the charge-carrier mobility as high as 10 000 $cm^2\,(Vs)^{-1}$, which has also been confirmed by the THz time-domain spectroscopy (THz-TDS). THz-TDS is a non-contact and non-destructive measurement technique used to probe the intrinsic transport dynamics of conductive films. THz-TDS probes the spatially averaged conductivity of graphene without any physical contact and has been used extensively to study graphene on a wide range of relevant substrates such as Si, SiC, quartz, sapphire and polymers [40–46]. Furthermore, our devices showed very low leakage currents and reduced gate-voltage-sweep hysteresis. This can be attributed to the absence of a sacrificial polymer layer during the transfer of graphene to the EVA/PET. The electronic properties of graphene induced by its electronic band structure leads to unusual effects, such as massless Dirac fermions and quantum Hall effect (QHE) [47, 48]. We report on arguably the first flexible graphene devices in which QHE has been observed in a relatively small magnetic field of 5–6 T. We believe that this method is an excellent contender to become a reference platform for RF-electronics, sensors, and optoelectronics, with further development.

1.1. Experimental methods

CVD graphene on copper was purchased from Graphenea or Sigma Aldrich or synthesized in-house in an AIXTRON Black Magic II cold-wall CVD system. A commercial system (SCS) was used to deposit Parylene N (see Supplementary Information, SI, for details) on CVD graphene on copper foil, which was temporarily attached to Si substrates for easier handling. This was followed by patterning a 110 nm thick gate electrode (Ti/Au/Ti = 5/100/5 nm) on Parylene N using standard photolithography, e-beam evaporation, and a lift-off process in sequence. Ti was used to improve the adhesion of the gate electrode to Parylene N and EVA [49]. The copper foil was eventually released from the Si carrier. Subsequently, the gate/Parylene/graphene/copper stack was laminated onto the EVA/PET foil in an ordinary office laminator [50]. Graphene was separated from the copper foil using the electrochemical delamination method in NaOH solution [51]. The resulting stack was again coated with Parylene N to fully encapsulate the graphene and prevent graphene contamination from subsequent lithographic processing. The final device patterning process proceeded with the formation of electrical contacts and etching of the Hall-bar shape of the graphene layer. Electrical contacts to graphene were fabricated using a two-layer resist stack (LOR1A and S1813). The oxygen plasma etching of the top Parylene layer revealed the graphene edge, which could then be contacted through the deposition of metal layers at an angle of 45 degrees while simultaneously rotating the sample at 5 rpm. This resulted in edge contacts showing specific contact resistance of $\sim$6 kohms·μm measured using transfer line method (see SI). This is in contrast with traditional edge contacts reporting very low specific contact resistance of $\sim$100 ohms·μm [52, 53]. This difference in the contact resistance can be explained by the flexible nature of our substrates, leading to mechanical deformations of contacts during bending of the samples. Finally, photolithography and oxygen-plasma etching were used to pattern the graphene channels into the Hall-bar geometry. A Schematic illustration of fabrication steps for the bottom-gated GFETs is shown in figure 1(a).

GFETs with a top gate were fabricated by first laminating graphene on copper onto EVA/PET foils [54]. Then, graphene was patterned, and Parylene N was deposited on the etched Hall bar structure. The device patterning was the same as that described above for the bottom-gated GFETs. Finally, a 110-nm thick gate electrode was patterned (Ti/Au = 10/100 nm) on Parylene N using standard photholithography, e-beam evaporation, and lift-off process in sequence. A schematic illustration of the fabrication steps for the top-gated GFETs is shown in figure 1(b).

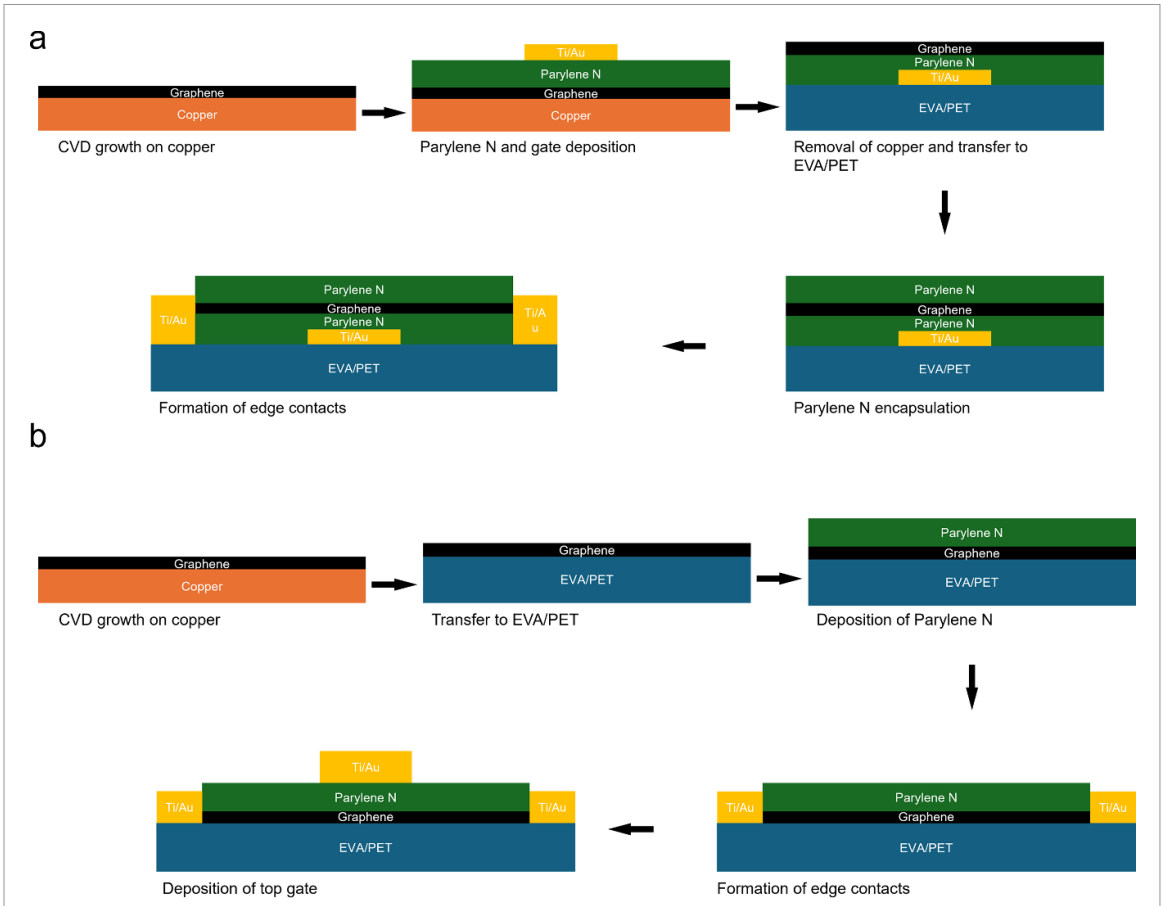

Figure 1. (a) Schematic of fabrication process of (a) bottom-gate GFET (b) top-gate GFET.

To prepare devices without a gate, CVD graphene laminated to EVA/PET was shaped into Hall bars using photolithography and oxygen-plasma etching. This was followed by the deposition of metal contacts followed by lift-off, using a similar electrode stack as before.

The Raman spectroscopy measurement was performed using the Horiba Raman XploRA ™ microscope with a 638 nm laser and a 100 × objective using 1200 gratings per mm and a 300 μm wide slit. The Zeiss Supra 55VP system with 5 kV accelerating voltage was used to acquire scanning electron microscope (SEM) images of the samples.

2. Results and discussion

CVD graphene transferred on EVA/PET and Parylene N was characterized by Raman spectroscopy and SEM. For this, three samples were prepared: (i) graphene on EVA/PET, (ii) graphene sandwiched between EVA/PET and Parylene N, and (iii) graphene on top of Parylene N laminated to EVA/PET. Figure 2(a) shows a schematic of the different configurations. Typical Raman spectra are shown in figure 2(b). The graphene G and 2D Raman peaks are located at $\omega_G = 1585$ 1/cm and $\omega_{2D} = 2635$ 1/cm for samples (i) and (ii). For sample (iii), the peaks are located at $\omega_G = 1574$ 1/cm and $\omega_{2D} = 2602$ 1/cm, respectively. The shifts in the peak positions can be explained by the different doping and strain in the graphene samples [55]. The D-peak is difficult to isolate due to overlapping bands of EVA and PET. The Raman spectrum showed a high I(2D)/I(G) ratio and a narrow symmetric 2D band, providing the first evidence of the high structural quality of the transferred CVD graphene. It was previously shown that random strain variations on the nanometer scale is the main source of the broadening of the Raman 2D peak, and that the low values of the full width at half maximum (FWHM) of the 2D peak are a direct indication of a uniform strain landscape within the laser spot [56]. The random strain variations resulting in the broadening of the 2D-peak were correlated with a low carrier mobility in graphene devices encapsulated in hBN [39]. SEM images of graphene on EVA/PET- and Parylene N (figures 2(c) and (d), respectively) reveal clearly visible multilayer patches (darker regions) and grain boundaries, which are typical for CVD graphene grown on copper foils.

Hall effect mobility measurements were performed at a perpendicular magnetic field strength of B = ±0.16 T in a four-terminal configuration (see SI for details). The measured Hall mobility μ_H and charge-carrier density n_s are shown in figure 3 for different sample layouts (insets). For top-gate-, bottom-gate-, and no-gate GFETs, the

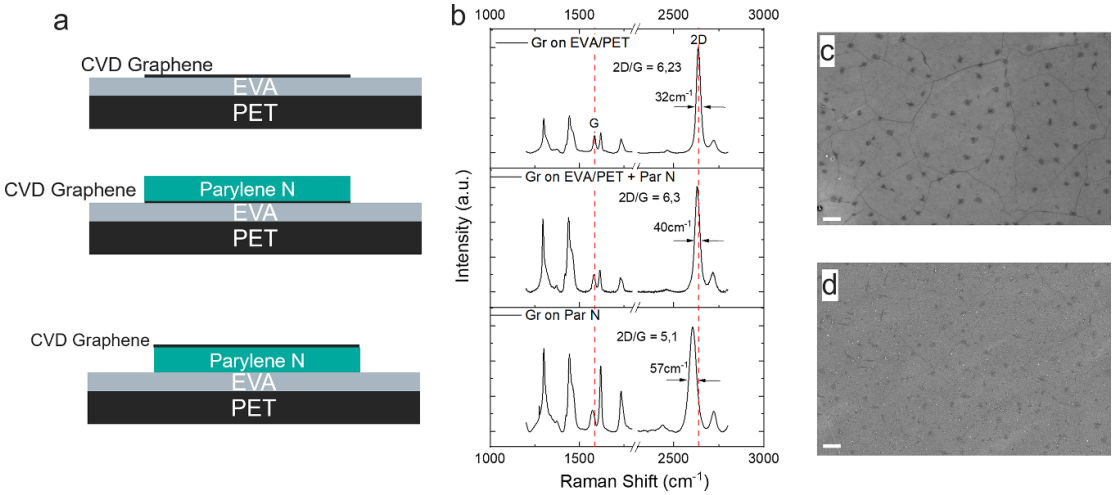

Figure 2. (a) Schematic of the sample preparation. CVD graphene was transferred to the EVA/PET via hot-press lamination. Parylene N was deposited by CVD. (b) Representative Raman spectra of CVD graphene for the schematic shown in panel (a). SEM pictures of CVD graphene on EVA/PET (c) and on Parylene N (d), respectively (the scale bar is 4 μm).

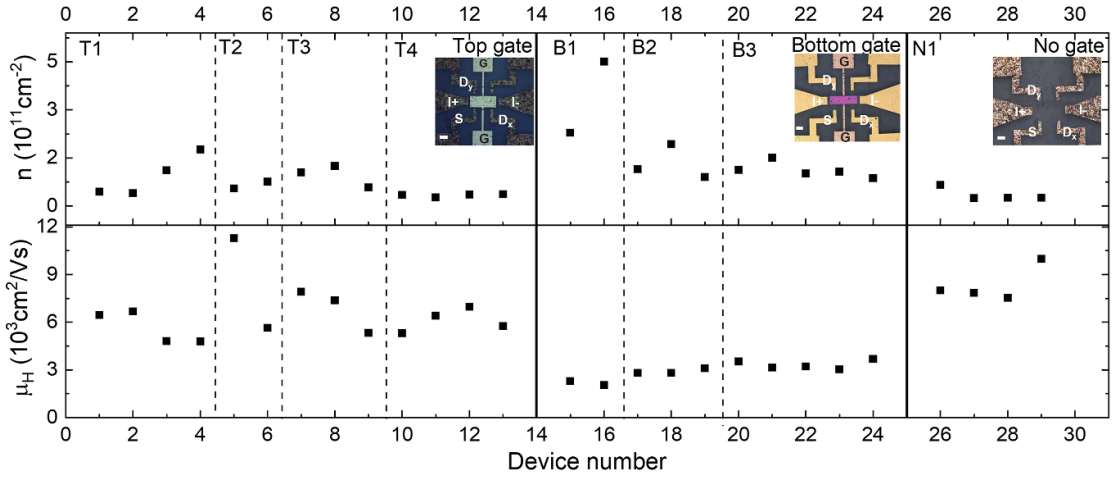

Figure 3. Hall-effect mobility and carrier density for the top-gated GFETs ('top gate'), bottom-gated GFETs ('bottom gate'), and graphene transferred to EVA/PET with no gate ('no gate'). Solid vertical lines separate the top, bottom, and no gate devices. The dashed vertical lines separate the devices fabricated in different batches. The inset shows optical images of the devices of respective configurations (scale bars are 75 μm).

average mobility was 6300 ± 1700, 2900 ± 500, and 8100 ± 1100 cm^2 (Vs)$^{-1}$, respectively. In agreement with the Raman spectra, the lower mobility observed in the bottom-gated GFETs is correlated with a lower I(2D)/I(G) ratio and a larger FWHM of the 2D peak. The lower μ_H for bottom-gated GFETs may be associated with the materials in contact with graphene (Parylene N compared to EVA/PET) as well as differences in the fabrication routes used (see section 1.1). In contrast, Parylene N on top of graphene transferred to EVA/PET does not seem to degrade the device properties.

To validate the robustness of our fabrication process, we fabricated devices in different batches (indicated by the dashed vertical lines in figure 3). Graphene from different vendors and graphene grown in-house on copper foils with different surface morphologies and thicknesses were used to fabricate the GFETs (see SI for details). The surface roughness of the fabricated GFETs in the top-, bottom-, and no-gate configurations is inherited from the topography of the copper foils. Despite some sample-to-sample variations, the overall charge-carrier mobility in our samples was consistently high. We would also like to highlight that our technique appears to be insensitive to the copper-foil surface morphology, as a high charge carrier mobility in graphene is observed for different copper foils used [57].

Several key metrics can be used to characterize the performance of a GFET. While particular efforts have been focused on improving the field-effect mobility [58–60], real-world applications also have stringent requirements for stable and consistent operation. Therefore, gate hysteresis, unintentional doping, and long-term instability are crucial parameters that must be minimized for graphene application in electronics

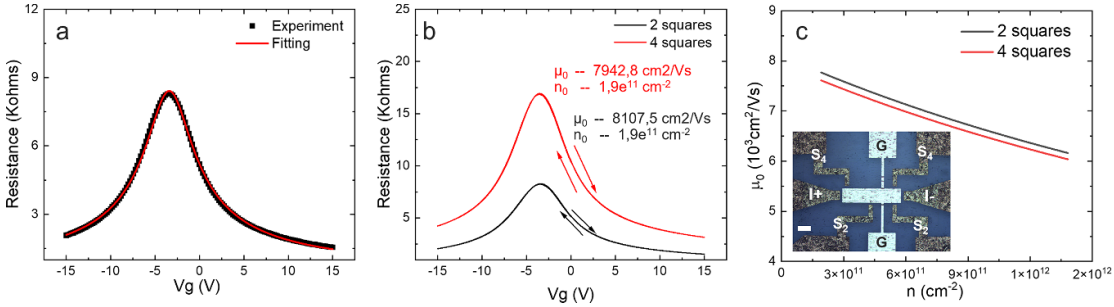

Figure 4. Fitting of $R(V_g)$ experimental curves to extract the field-effect characteristics. (a) A typical plot of the four-terminal resistance of graphene, R, as a function of the gate voltage, V_g, measured at room temperature and fitted by the model represented by equation (1). (b) Forward and backward voltage sweeps for top-gated GFETs with the channel aspect ratio (L/W) = 2 and 4. (c) The field effect mobility as a function of carrier density extracted by using equation (2). The inset shows the optical image of the top-gated GFETs (scale bar is 75 μm).

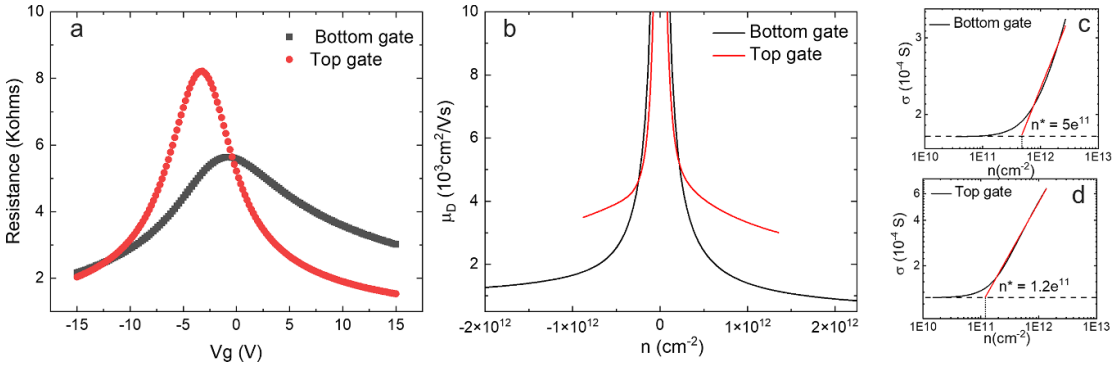

Figure 5. (a) Transfer characteristics of the top-and back-gated GFETs. (b) Drude mobility vs. charge carrier density for the top- and bottom-gated GFETs. (c) and (d) Procedure to extract n^* from the log-log $\sigma(n)$ plots.

and optoelectronics. Figure 4(a) shows the four-terminal resistance measured as a function of the gate voltage V_g; also shown is a fit to the modified model by Jeppson *et al* [61] represented by equation (1) to extract the charge-carrier mobility and residual density

$$R_{\text{total}} = \frac{1}{k\sqrt{n_0^2 + n\left(V_g\right)^2}} + \frac{\theta}{k} + R_{\text{co}}, \qquad (1)$$

Here, $k = (W/L)\mu_0 C_{\text{ox}}$, is the transconductance parameter, n_0 is the density of residual charge carriers at the minimum conductivity (Dirac) point, μ_0 is the long-range Coulomb scattering charge-carrier mobility, $W = 75$ μm, $L = 150$ μm and 300 μm for the channel aspect ratio $(L/W) = 2$ and 4, respectively, θ is the mobility degradation parameter, $n(V_g)$ is the gate-induced charge-carrier density, q is the electron charge, and C_{ox} is the gate oxide capacitance per unit area for a Parylene N thickness of 200 nm and dielectric constant of 2.65. C_{ox} can be found from the gate-dependent Hall effect measurements (see SI). R_{co} is the sum of the drain and source contact resistances, including the access areas between the metal contacts and channel not covered by the top gate. All resistance measurements were performed using a four-terminal configuration, eliminating the contact resistance, $R_{\text{co}} \approx 0$. Figure 4(b) shows the transfer curves and the extracted properties (n_0, μ_0) of the devices of different lengths (see the inset of figure 4(c)), alongside the hysteresis-free transfer curves for the forward and backward gate-voltage sweeps. Figure 4(c) shows the extracted hole mobility given by equation (2) as a function of the charge-carrier density $n = \frac{C_{\text{ox}}}{q}\sqrt{n_0^2 + n(V_G)^2}$

$$\mu = \frac{\mu_0}{1 + n/n_{\text{ref}}}, \qquad (2)$$

where $n_{\text{ref}} = C_{\text{ox}}/(q\theta)$ is the carrier density for which the mobility is reduced to one-half of its initial value (μ_0). The dependence of the mobility on the charge carrier density can be obtained from the measurements, where the Hall mobility is traced as a function of V_g (see SI). Figure 5(a) shows the transfer curves, $R(V_g)$, at room temperature for the GFETs with top and bottom gates. The mobility of each sample is extracted by performing fits, as in figure 4(a). All the devices (the top- and bottom gate) are of the same dimensions, $W = 75$ μm and $L = 150$ μm. Parylene N thickness for the top-gate- and bottom-gate devices is 200 ± 20 nm and 120 ± 12 nm, respectively. For the samples shown in figure 5(a), we obtain

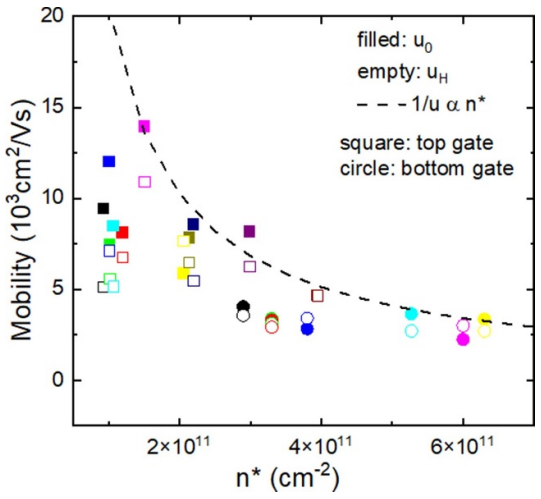

Figure 6. Mobility versus disorder-induced charge-carrier fluctuations n^* in graphene samples. Field (solid squares) and Hall effect (empty squares) mobilities for the top (square) and bottom (circles) gated GFET's. Different colors refer to the field and Hall effect mobilities of different devices. The dashed line corresponds to the model in [65], which describes the inverse proportionality between μ and n^*.

$\mu_0 = 2247$ cm^2 (Vs)$^{-1}$ for the bottom-gated GFET and $\mu_0 = 8107$ cm^2 (Vs)$^{-1}$ for the top-gated GFET in reasonable agreement with the Hall mobility μ_H for the same devices (3000- and 6740 cm^2 (Vs)$^{-1}$, respectively). The asymmetry of the p- and n-sides of the transfer curves for the bottom-gated GFETs can be explained by different scattering cross sections of electrons and holes on charged impurities [62, 63] unintentionally introduced during device fabrication and/or due to exposure to ambient conditions. In figure 5(b), we show the mobility calculated according to the Drude model $\mu_D = \sigma/(ne)$, as a function of n for the GFETs with top and bottom gates, where σ is the electrical conductivity of graphene. At a high carrier density, μ_D may decrease due to supercollisions involving defects [64]. Another indicator of sample quality is given by disorder-induced fluctuations in charge carrier density n^*. This quantity provides a measure of the potential fluctuations experienced by electrons [65]. This can be extracted by plotting $\sigma(n)$ on a double logarithmic scale (figures 5(c) and (d)). In figure 6, we analyze the correlation between the mobility and n^*. We do so by considering both the long-range Coulomb scattering mobility μ_0 (solid squares) and the Hall mobility μ_H(empty squares). μ_0 and μ_H showed a reasonable agreement for all devices, corroborating the discussion above. The general behavior is well described by the relation $\mu \propto 1/n^*$ [65] (see the dashed line in figure 6). We can conclude that our fabrication technique and architecture consistently result in graphene devices with statistically much higher mobility and smaller potential fluctuations than in those fabricated using the wet transfer method and Si/SiO$_2$ substrates. The fabricated devices exhibit remarkable long-term stability when exposed to ambient atmosphere and nitrogen (see SI).

Magnetotransport measurements were performed to further examine the device quality. Figure 7 shows the longitudinal magnetoresistance R_{xx} and the Hall resistance R_{xy} as a function of the magnetic field B. Both dependencies demonstrate the characteristic signatures of QHE): a vanishing $R_{xx}(B)$ and the appearance of a plateau in $R_{xy}(B)$ in a certain range of $B > B_{onset} = 5 - 6$ T. For the top-gated GFET (figure 7(a)) we found $B_{onset} < 5$ T for the filling factor $\nu = 2$ at $V_g = -6$ V and for samples transferred to EVA/PET (figure 7(a)) $B_{onset} \approx 4$ T, both at 2 K. We also performed magnetotransport measurements for samples transferred to EVA/PET at higher temperatures (figure 7(b)). The QHE features were observed at temperatures as high as 100 K (see figure 7(b)) in these samples. However, R_{xy} in the plateau region is not exactly equal to $h/(2e^2)$ and R_{xx} is not exactly zero. This behavior has previously been explained by the presence of grain boundaries and multilayer patches in CVD-based devices [66]. To the best of our knowledge, this is the first observation of QHE in graphene on a flexible polymeric substrate. We also note that our devices are one order of magnitude bigger (250-μm-long graphene channel) compared to experiments where QHE was observed in CVD graphene encapsulated in hBN [39, 67, 68], which could be an indicator of high uniformity on a large scale.

To further provide insight into large-scale uniformity, we employed THz-TDS, which is a well-established method for characterizing the electrical properties of graphene on to m^2 scale [42]. In this work, THz-TDS was carried out using a fiber-coupled spectrometer system (TOPTICA Teraflash Pro) described in detail elsewhere [42]. For transmission mode measurements, the samples were raster-scanned in 200 μm steps in the focal plane between the emitter and detector to form spatial signal maps, with the spot size being of order 0.3 mm (at 1 THz). The DC conductivity, charge carrier mobility and density were extracted from the maps of the cm^2-large graphene films. Three samples $\sim 1 \times 1$ cm^2 large were prepared for the THz-TDS measurements, with CVD graphene transferred to EVA/PET, to Parylene N, and encapsulated in Parylene N, as shown in figures 8(a)–(c), respectively. The frequency-dependent sheet conductivity of graphene, $\sigma_s(\omega) = \sigma_1 + i\sigma_2$, was calculated at each point of the scanned maps from the transmission function $T_{film}(\omega) = (1 + n_{sub})/(1 + n_{sub} + Z_0\sigma_s(\omega))$ for a substrate with refractive index n_{sub}, where Z_0 is the vacuum impedance [41, 42]. The measured frequency-dependent conductivity was fitted with the Drude model using the DC conductivity σ_{DC} and Drude scattering time τ as fitting parameters

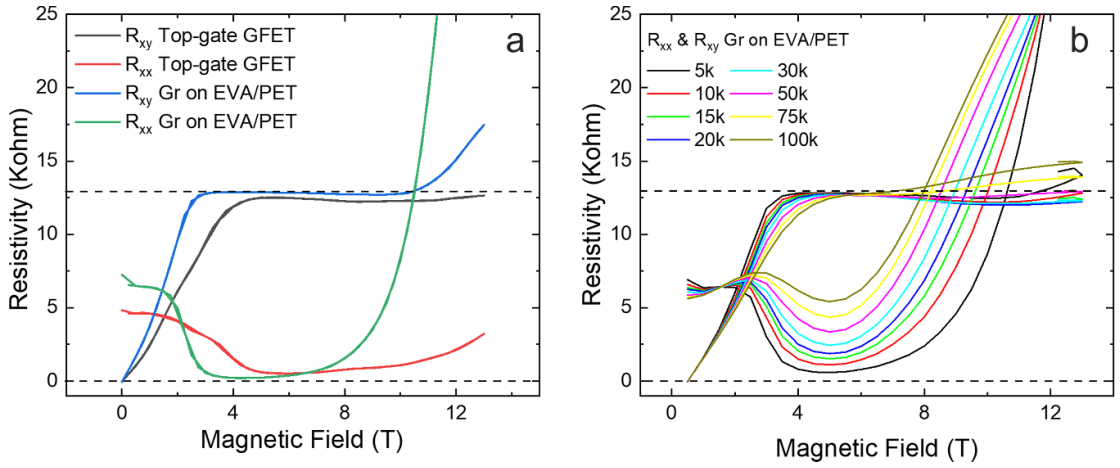

Figure 7. Quantum Hall effect observed (a) in the top-gated GFET and bare graphene transferred to EVA/PET measured at 2 K and (b) at different temperatures for graphene on EVA/PET. The top and bottom horizontal dashed lines represent the resistivity values of 12 941 Ω- and 0 Ω, respectively.

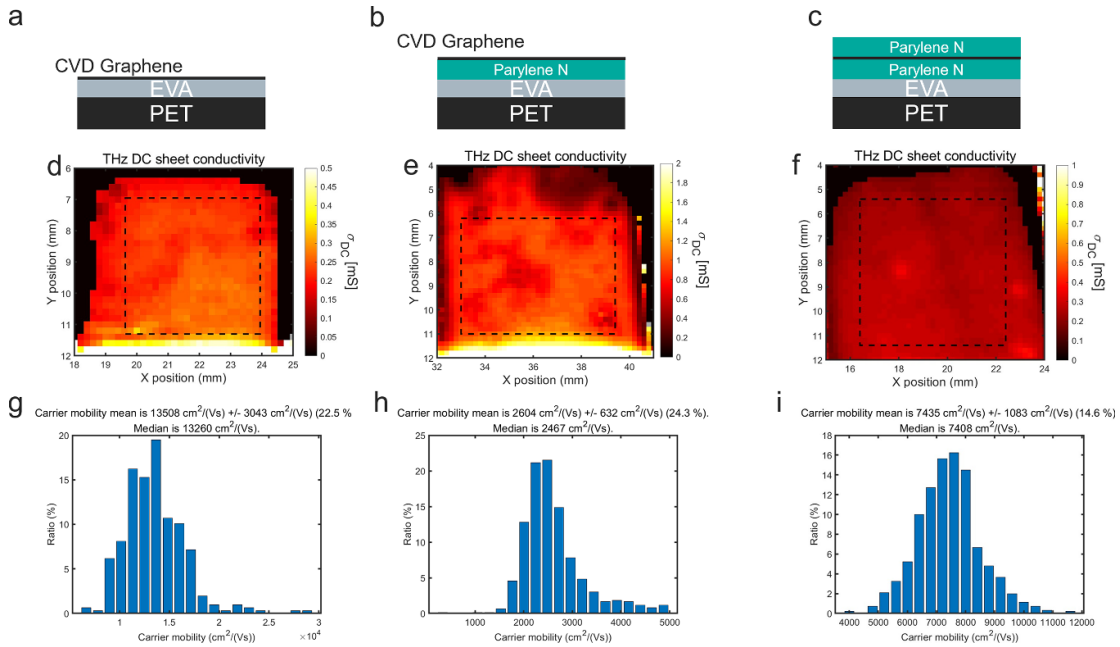

Figure 8. Different sample structures of CVD graphene transferred to (a) EVA/PET, (b) CVD graphene transferred on Parylene N, and (c) CVD graphene encapsulated in Parylene N. (d)–(f) Corresponding THz DC conductivity maps. (g)–(i) Corresponding histograms of the charge-carrier mobility. The black dashed boxes in the maps represent the areas from which mobility histograms were extracted.

[42]. Assuming that the transport can be described using semi-classical transport theory [69], the density and mobility are calculated as in reference [42]. Previous studies have shown a good agreement between the electrical measurements using THz-TDS and Hall- or field-effect measurements on CVD graphene [42, 43, 70]. The conductivity maps of our graphene samples are shown in figures 8(d)–(f). Histograms of the carrier mobility for each sample in figures 8(g)–(i) are extracted from the data points inside the dashed-line rectangle in figures 8(d)–(f). The THz-TDS results were in good agreement with the Hall- and field-effect measurements. The higher mobility values measured for samples using THz-TDS can be attributed to a sample-to-sample variation and the fact that no further processing (photolithography) was done on these samples, which usually leads to some contamination and, hence, worse transport properties. We also measured the THz-TDS on the samples encapsulated in Parylene N and report on three times higher charge-carrier mobility compared to the samples transferred onto Parylene N (before the encapsulation). The encapsulation contributes to the long-term stability and protection of devices from humidity and contamination [71] and protection against mechanical damage, leading

to a significantly higher carrier mobility than that reported for other scalable graphene encapsulation strategies, including atomic layer deposition [58].

3. Conclusion

In summary, we presented excellent electrical transport properties for CVD graphene when transferred onto EVA/PET. The transport characteristics are similar to those of equivalent samples composed of micrometer-sized graphene flakes on Si/SiO_2 substrates. In particular, our devices exhibited room-temperature charge-carrier mobility up to 10 000 $cm^2 (V s)^{-1}$ and QHE up to 100 K.

We used Hall-effect, field-effect, and THz-TDS measurements to assess the transport properties of our samples, which allowed us to confirm the high uniformity, consistency, and quality of the electrical properties with great certainty. Using a straightforward, highly scalable fabrication process, we have shown that graphene on flexible substrates can not only compete but may even surpass the state-of-the-art for graphene on fixed solid substrates, in terms of the electrical performance of large-scale devices.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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Conflicts of interest

There are no conflicts of interest to declare.

ORCID iDs

Munis Khan https://orcid.org/0000-0002-9654-0014
Peter Boggild https://orcid.org/0000-0002-4342-0449
August Yurgens https://orcid.org/0000-0002-3038-1911

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