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Thesis for the degree of Doctor of Philosophy

Design, Modelling and Implementation of High Power Density Drive for Electric Vehicles

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Abstract

The world is facing an unprecedented ecological crisis due to our ever increasing demand for energy. Today roughly 37% the total CO2 emissions are generated by transport. In the last decade transportation electrification has seen a large push. This way it is possible to eliminate local emissions and if the electricity generation is CO2 neutral also the global emissions.

Some of the main challenges of electric vehicles are range and cost. Apart from declining component cost, especially of the battery packs, important factors of the electric vehicle drive-train are efficiency and size. With increased efficiency the cooling system of the drive-train can be smaller and thus the system size and mass can be further decreased. Further drive-train downsizing can be achieved by integrating the inverter and electric motor and utilizing new wide band-gap semiconductors such as SiC.

To understand the design process first the vehicle requirements and dynamics need to be understood. Electric vehicle system architecture is therefore first presented in this thesis. Once the global requirements are taken into account, the inverter design can be performed. Further, an easy to use estimation tool of the inverter losses is required to understand the cooling requirements and feasibility of the design. Therefore, the second part of this work focuses on loss modelling of inverters and semiconductors. Next, the DC link capacitors are discussed and the dimensioning processes are presented. This work investigates the possibility of utilization of a double-three-phase topology (DTP) to reduce the DC capacitor bank of the inverter. This is achieved by means of carrier wave interleaving which makes it possible to reduce the capacitor current stress. This modulation technique makes it also possible to optimize for the capacitance rating of the capacitor bank. The DTP topology is then utilized when designing a low C-rate inverter for an $800\,\mathrm{V}$ traction system. The adopted DC link capacitor bank is $23.5\,\mu\mathrm{F}$.

Aluminium substrate printed circuit boards with high thermal dissipation characteristics are investigated as an alternative to SiC power modules. The Al-PCB concept utilizes surface mount devices which are generally cheaper and more available as well as inhibit a higher degree of flexibility for the designer. This makes it possible to mount temperature sensors and current sensors on the Al-PCB increasing the power density further. The flexibility offered by Al-PCB can be exploited to adapt the inverter to the machine geometry for better integration. A prototype with the volume of $2.17\,\mathrm{L}$ is then experimentally verified in a prototype capable of delivering $250\,\mathrm{kW}$ for a DTP drive.

Keywords: Integrated, drive, electric, vehicle, SiC, metal, core, pcb, capacitor

Acknowledgments

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Last but not least I would want to thank Energimyndigheten and the European Commission for financially supporting this work.

Abbreviations

2L-VSI Two Level Three Phase Voltage Source Inverter

AC Alternating Current

Al-PCB Aluminium Substrate Printed Circuit Board

BEV Battery Electric Vehicles

DC Direct Current

DTP Double Three Phase

ESM End Stator Mounted

EV Electric Vehicles

EWM End Waterjacket Mounted

FEM Finite Element Method

GaN Gallium Nitride

HEV Hybrid Electric Vehicles

ICE Internal Combustion Engine

IGBT Insulated Gate Bipolar Transistor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NTF No Thermal Feedback

PCB Printed Circuit Board

PMSM Permanent Magnet Synchronous Machine

PWM Pulse Width Modulation

RMS Root Mean Square

RSBM Radial Stator Back Mounted

RWM Radial Waterjacket Mounted

SiC Silicon Carbide

SMD Surface Mount Device

THD Total Harmonic distortion

TIM Thermal Interface Material

VSI Voltage Source Inverter

W-RC With Reverse Conduction

W-RC With Reverse Conduction

WBG Wide Band-Gap

WTF With Thermal Feedback

Contents

CHAPTER 1

Introduction

1.1 Background

The effects of global warming are now being observed world wide. One of the main driving factors behind this phenomenon is the consumption of hydrocarbons for heat, power generation and mobility, resulting in the emission of CO2 [1]. In the EU, the transportation sector was responsible for $25\,\%$ of the total greenhouse gas emissions [2]. Therefore, there is a consensus in the scientific community that these emissions must be radically reduced [3]. Additionally there is a political push, for example by the EU to reduce transportation emissions by up $95\,\%$ by 2050 compared to the 1990 level [4]. Therefore, transportaion electrification is a necessery step to reducing the total greenhouse gas emissions. Recently, passenger vehicle electrification has increased, constituting $46\,\%$ of total passenger vehicle sales [5]. Despite recent years' uncertain times such as COVID-19, passenger EV sales are experiencing an exponential trend, as seen in Fig. 1.1. From most recent sales figures, BEVs and HEVs are becoming adopted by the public as a reasonable alternative for personal mobility. Li-ion batteries are used as energy storage devices in a BEV, whereas in an HEV, fossil fuels and Li-ion batteries are used. The increased sales of BEVs can be attributed to the aggressive taxation of ICE-driven cars [6], with the radical price decrease of the

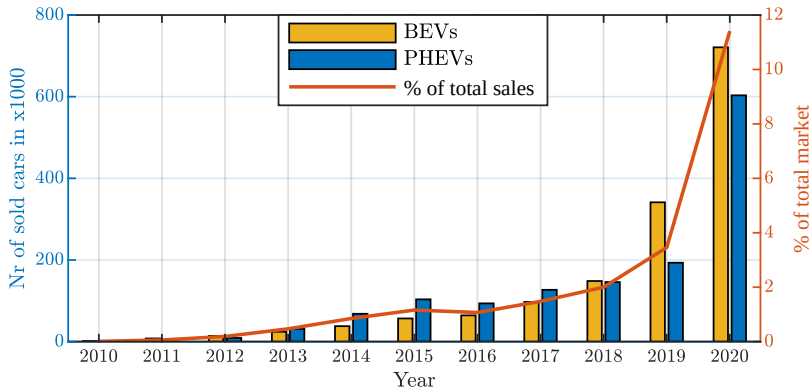


Figure 1.1: Sales of electrified vehicles in the EU from 2010 through 2020 in absolute numbers and in relation to total vehicle sales [9]

Li-ion battery packs [7], the vehicle's most expensive component by far [8].

The drive train of an electric vehicle consists of the energy storage device, the inverter, the electric machine, and the transmission. Most commonly, the energy storage device is a Li-ion battery. A schematic depiction can be found in Fig. 1.2. The gearbox in electric vehicles is commonly fixed-speed and sometimes two-speed, which significantly reduces complexity compared to the ICE counterparts. The electric motor is an AC machine driven by an inverter that controls the supplied power to the machine from the battery. Auxiliary electric equipment such as a charger and a 12V electric system is also present. Two of the challenges EVs face is the reduced driving range compared to ICE due to the low energy density of Li-ion batteries and higher starting costs [8]. Although incorporating more Li-ion batteries can improve the driving range, it adds to the cost. An alternative is to physically integrate the drivetrain's various sub-systems, e.g., electric machine and inverter [10], [11]. Such a solution has the potential to reduce weight using shared housing and cooling. Furthermore, the cost can be reduced by optimizing the designs of the sub-systems and employing designs that can enable automated manufacturing.

Research questions

The inverter shown in Fig. 1.3 is used as a propulsion inverter. Although various topologies, e.g., multi-level, are proposed in the literature, a 2-level voltage source

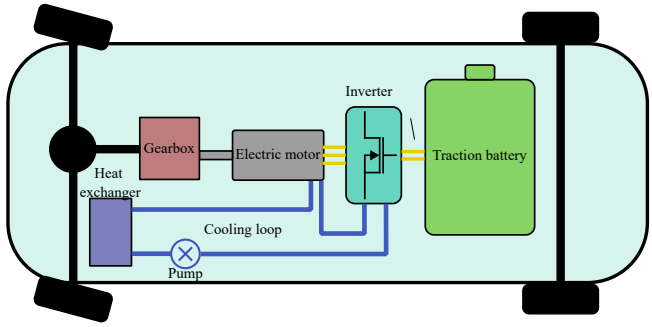


Figure 1.2: Schematic overview of the constituting components of an electric drive train in an EV.

converter (VSC) is the most used propulsion inverter for EV applications [12], [13]. As shown in Fig.1.3, the inverter consists of the power semiconductors, the DC link capacitor bank, and the heatsink. Additionally, copper bus bars are used to connect DC link capacitors to the power semiconductors and loads to the semiconductors. Furthermore, gate driver/control boards supply the gating pulses to control the semiconductor switches and sensors for measurements. This thesis explores the design optimization of a propulsion inverter to achieve integration with the electric machine and reduce cost via design for manufacturing.

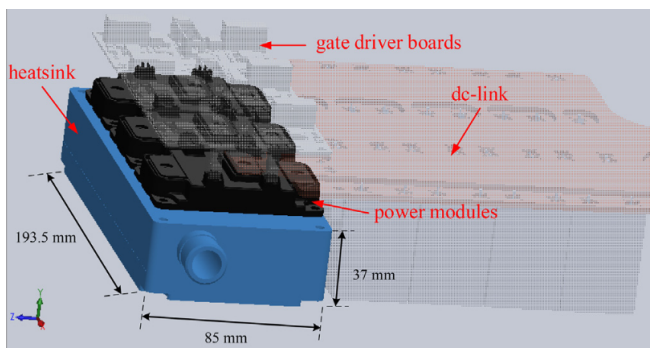


Figure 1.3: CAD of a high power inverter with a film capacitor bank [14].

The heat generated by the switching actions of the semiconductors needs to be transported away to the coolant medium in the most efficient way possible to avoid

overheating of the devices. One way to reduce the cooling requirements is by utilizing low loss WBG devices, e.g., SiC, GaN which are more expensive compared to conventional Si based devices [15]. Another way is by an over-design of cooling capacity that is often employed to guarantee safe operating conditions which leads to additional weight. Alternatively, the heat sink design can be optimized by undertaking a system level optimization approach e.g., using drive cycle [14], [16]. Finite element thermal simulations are commonly utilized to estimate the cooling requirements of inverters [17]. To effectivize this process, accurate and easy to use loss estimation tools are required that can be employed in system level studies e.g., using drive cycles and life time estimations models [16].

The power semiconductor devices used in the inverter are often arranged as module with several switches connected in parallel to achieve the required load current requirements [18]. The layout of the semiconductor chips inside the module are optimized by the manufacturer [19]. However, the additional design optimization of the layout, interfaces and module housing incurs additional cost compared to discrete devices of the same rating. As can be seen in the Fig. 1.3, these modules are mounted on the heatsink using screws which increases the manufacturing steps of the inverter. Inverter designs with discrete semiconductor components can be used as an alternative to modules [20], [21].

Traditionally discrete components in highly power dense applications is challenging due to relatively poor cooling performance of the discrete packages in combination with the available PCB technology. A one layer PCB has been verified in a low voltage high current application [20] for EVs. In another study a $600\,\mathrm{V}$ system is experimentally verified in a low current application [22]. However, in both cases the thermal management system is not optimized nor is a two layer Al-PCB explored as an alternative for a high current, high voltage direct cooled traction application for EVs.

The DC link capacitors are a major component in terms of volume, as can be seen in Fig. 1.3. The DC link capacitors can often occupy more space in comparison to semiconductors and heatsink in the inverter [23]. The big size of these DC link capacitors can limit integration with machine due to space constraints and the environmental requirements of the capacitors. Therefore, reducing the size of the DC link capacitors is necessary to improve the volumetric power density and easier integration. The DC link capacitors provide a power buffer and absorb the ripple current generated by the switching action of the semiconductor devices. In practice, the active power is supplied by the DC side of the inverter whereas the reactive power is stored in the

capacitor bank [24]. The necessary capacitance to maintain the voltage ripple within specification levels can be reduced by increasing the switching frequency, which is possible when using wide bandgap devices [25]. Alternatively, the size could also be reduced by using multi-phase configuration as it is possible to implement carrier wave interleaving and the output currents of the multi-phase machines are out of phase with each other, which can further reduce the capacitor size. Reseach in this area has already been undertaken however only case studies have been presented and no full operating maps have been investigated [26]. Therefore, an analysis of the DC link capacitor voltage and current stress in a DTP 2-level inverter is needed.

There are three main types of DC link capacitor technology suitable for inverter application: electrolytic, film and ceramic [27], [28]. Electrolytic capacitors typically offer high capacitance rating and low current rating. Therefore, they used to be utilized when high switching frequencies were hard to achieve. Nowadays IGBT and SiC offer sufficiently high switching frequency; therefore, electrolytic capacitors are not preferred in inverters for modern EV applications. Film capacitors offer moderate capacitance levels and moderate to high current carrying capabilities. Hence are the capacitor of choice for modern EV applications. One of the main drawbacks of film capacitors is their temperature sensitivity and they rarely can operate above $100\,^{\circ}\mathrm{C}$, hence not being a suitable technology for SMD technology. Ceramic capacitors are typically featured as a decoupling and filtering device due to their low capacitance level but fast dynamics. Some of the main advantages of ceramic capacitors feature high current rating and high temperature capability. Typically current carrying capability and insulation level (voltage tolerance) are inverse capabilties of capacitors. An overview of typical applications of the capacitor technologies based on voltage level and capacitance can be seen in Fig. 1.4. In practical applications further considerations such as bus bar mounting have to be made. Some semiconductor packages have special made capacitor modules [29]. If not available a distributed approach has to be taken [30]. In the latter a greater flexibility is achieved at the expense of power density. Ceramic capacitors can due to their temperature stability be directly soldered onto the power PCB, which also enables improved cooling. Due to the low C-rating of ceramic capacitors however, are rarely employed in capacitor bank applications at typical traction voltages of $400\,\mathrm{V}$. However, by utilizing high switching frequency WBG devices as well as DTP topology could reduce this requirement and should be studied.

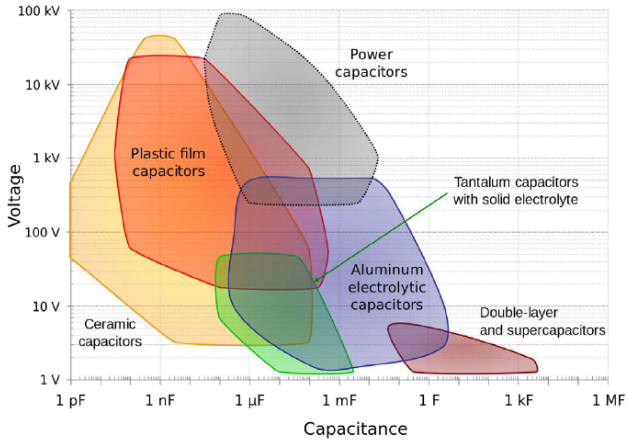


Figure 1.4: Overview of capacitor technologies and their operating regions [31].

Research contribution

In this thesis, analytical loss calculation methods are proposed and evaluated for faster estimation of semiconductor losses. A 6-phase configuration and higher switching frequency is utilized to reduce the size of DC link capacitor. Additionally, ceramic capacitors are used in the DC-link instead of film capacitor to improve ease of manufacturing. Furthermore, the inverter is designed using discrete semiconductor switches mounted on an aluminium substrate.

An improved analytical loss calculation methods considering the reverse conduction and blanking time is proposed. The loss estimation method is verified using a 2L-VSI with SiC MOSFETs in a double jacketed caloriemtric box where the coolant flow and temperatures are measured. The results of the measurement show that the proposed method has a small error of $1.5\,\%$. In addition a parameter sensitivity analysis is performed with regards to device junction temperature. It is verified against simulations using Matlab/PLECS numerical software package.

A dimensioning method for DC link capacitors in a DTP inverter is proposed. The DC link current and voltage stresses are modelled using a numerical simulation method and is benchmarked against known three phase cases. Upon expanding this method to DTP topology it is found that the current and voltage stress can be influenced by both phase offset as well as PWM carrier wave offset. It is found that the capacitor bank current stress can be decreased by up to $38\,\%$ and voltage stress

45 % compared to a three phase equivalent.

As a result of the above research outcomes if higher switching frequencies (50 kHz) are utilized, ceramic capacitors can be utilized in 800 V traction voltage system if a DTP topology is utilized. Which result in a low capacitance design of roughly 23.5 µF. An Al-PCB substrate is decided for due to its high thermal dissipation capabilities and possibility to utilize direct cooling. Since this is a PCB in the traditional sense, high volume production automatizing is possible on a single substrate incorporating capacitors and semiconductors, resulting in the additional benefit that the capacitors are well cooled. The Al-PCB is a two layer substrate utilizing flux cancellation and high thermal conductivity dielectric material. To further improve the thermal characteristics of the Al-PCB thermal vias are used to thermally bypass one of the dielectric layers. This concept is prototyped for a 250 kW inverter. Thermal verification experiments show that this SiC based inverter can dissipate the losses which are produced when delivering the nominal output power. As a result a low profile direct cooled inverter for integrated EV application is proposed.

1.2 List of publications

I A. Rodionov, F. Mannerhagen and Y. Liu, "Design and Parameter Sensitivity Analysis of a Heatsink for a Direct Cooled Power Module with a Ribbon Bonded Cooling Structure," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2019, pp. P.1-P.10, doi: 10.23919/EPE.2019.8915013.
Contribution: study design, FEM analysis, writing

II A. Acquaviva, A. Rodionov, A. Kersten, T. Thiringer and Y. Liu, "Analytical Conduction Loss Calculation of a MOSFET Three-Phase Inverter Accounting for the Reverse Conduction and the Blanking Time," in IEEE Transactions on Industrial Electronics, vol. 68, no. 8, pp. 6682-6691, Aug. 2021, doi: 10.1109/TIE.2020.3003586.
Contribution: model verification, study design, experiments, writing

III A. Rodionov, A. Acquaviva and Y. Liu, "Sizing and energy efficiency analysis of a multi-phase FSCW PMSM drive for traction application," IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 2020, pp. 2069-2074, doi: 10.1109/IECON43393.2020.9254544.
Contribution: study design, modelling, writing

IV A. Rodionov, X. Huang and Y. Liu, "Analysis of DC Link Current and Voltage Stress for Motor Drive Application in Dual Three-Phase Configuration," IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 2020, pp. 1267-1272, doi: 10.1109/IECON43393.2020.9255043.
Contribution: study design, modelling, writing

V A. Rodionov, N. Sharma and Y. Liu, "Sizing, Design and Verification of a High Power Density 800 V Propulsion Inverter Based on Metal Substrate PCB and SMD components," *TO BE PUBLISHED*, Contribution: concept, study design, modelling, experiments, writing

Further publications not included in the thesis

VI Kersten, A.; Rodionov, A.; Kuder, M.; Hammarström, T.; Lesnicar, A.; Thiringer, T. Review of Technical Design and Safety Requirements for Vehicle Chargers and Their Infrastructure According to National Swedish and Harmonized European Standards. Energies 2021, 14, 3301. https://doi.org/10.3390/en14113301
Contribution: study outline, review

VII N. Sharma, B. Jiang, A. Rodionov and Y. Liu, "A Mechanical-Hardware-in-the-Loop Test Bench for Verification of Multimotor Drivetrain Systems," in IEEE Transactions on Transportation Electrification, vol. 9, no. 1, pp. 1698-1707, March 2023, doi: 10.1109/TTE.2022.3191411.
Contribution: writing and article review

CHAPTER 2

Loss modelling of inverters

This chapter focuses mainly on two level VSI and their loss modelling. The most common VSI is the 2L-VSI. An example of such an inverter is depicted in Fig. 2.1. The input is typically a DC voltage, either from a rectifier stage or from a battery. The output is typically a symmetrical three phase load with inductive character - typically an electric machine. Between the input and the inverter stage there is typically a smoothing capacitor which has the purpose of clamping the voltage and providing the output with reactive power. The middle point of the capacitor can be indicated as a fictive zero point.

The active components consist of semiconductor switches, most commonly IGBTs or MOSFETs. The switching actions inhibit losses which in turn produce heat and if the thermal limit is reached the switches fail. Therefore losses and heat dissipation of the switches is a very important topic in power electronics. Estimating losses quickly and conveniently improves the final design. Therefore, it is important to have accurate analytical models which makes quick evaluation possible.

Losses in traditional IGBT/MOSFET based inverters can be split in on-state and switching losses. The inverter features also additional losses such as gate driving losses and losses during off-state. These can often normally be neglected when evaluating the performance of a high power inverter [32]. A map of individual power

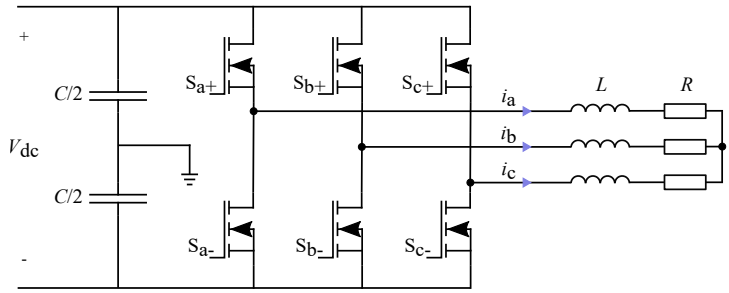


Figure 2.1: A two level three phase voltage source inverter

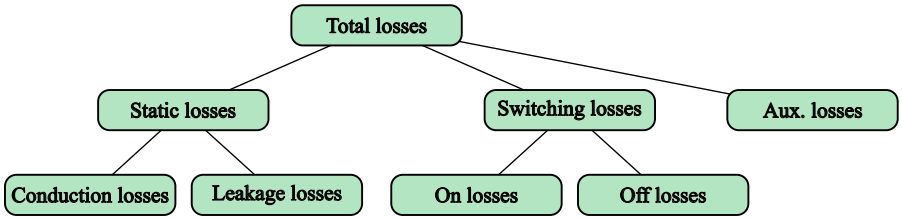


Figure 2.2: Map of loss components of an inverter

losses of the semiconductor stage can be seen in in Fig. 2.2. There two parts which contain the most loss are the static and switching losses. The semiconductors have a small leakage current while in the off-state which contribute to a normally negligible loss. While in the on-state the semiconductors feature a voltage drop which leads to a power loss which can be significant even at partial load operating points. The other significant loss component is the switching loss which occurs both when the switch turns on and off. Especially in IGBTs switching losses can be a thermally limiting loss component. The auxiliary losses such as gate driver losses can typically be neglected from a thermal packaging point of view.

Therefore, total losses of one switch are typically described as

$$P_{\mathrm{tot}} = P_{\mathrm{c}} + P_{\mathrm{sw}} \tag{2.1}$$

where P_{tot} is the total loss, P_{c} is the conduction loss and P_{sw} is the switching loss - the sum of the turn on and turn off losses respectively.

In the following sections the analytical loss modelling of IGBTs and MOSFETs are discussed. Analytical models are important for quickly drafting and selecting

relevant switches when in the design stage. Then a model for MOSFETs is suggested, experimentally verified and compared to its IGBT counterpart. Finally the MOSFET model is extended with thermally dependent parameters and a sensitivity analysis of these parameters on final losses is done.

2.1 Conduction losses in IGBTs

The conduction losses of an IGBT-based inverter bridge can be expressed as a sum of the loss through the IGBT and the diode as

$$P_{\mathrm{c}} = P_{\mathrm{c,T}} + P_{\mathrm{c,D}} \tag{2.2}$$

where $P_{\mathrm{c,T}}$ depicts the IGBT conduction loss and $P_{\mathrm{c,D}}$ is the diode conduction loss. The conduction loss in a two level PWM inverter supplying a sinusoidal output current depends on the modulation index as

$$M = \frac{\hat{V}_{\mathrm{out}}}{V_{\mathrm{dc}}/2} \tag{2.3}$$

where $\hat{V}_{\mathrm{out}}$ is the amplitude of the fundamental harmonic of the phase voltage and V_{dc} is the DC link voltage. When driving motor loads or other inductive loads the power factor is less than one, $\cos(\varphi) < 1$. Furthermore, the collector-emitter voltage, v_{CE}, across an IGBT mimics that of a diode and can be expressed as

$$v_{\mathrm{CE}} = V_0 + R_{\mathrm{on}} i_{\mathrm{T}} \tag{2.4}$$

where V_0 is the static voltage drop component and $R_{\mathrm{on}} i_{\mathrm{T}}$ is the dynamic loss component dependent on the on-state resistance and current magnitude. Considering this, the conduction losses can be expressed as

$$P_{\mathrm{c,T}} = \left(\frac{1}{2\pi} + \frac{M\cos(\varphi)}{8}\right) V_{0,T}\hat{I}_1 + \left(\frac{1}{8} + \frac{M\cos(\varphi)}{3\pi}\right) R_{\mathrm{on,T}}\hat{I}_1^2. \tag{2.5}$$

In an analogue fashion the anti-parallell diode conduction losses are described as

$$P_{\mathrm{c,D}} = \left(\frac{1}{2\pi} - \frac{M\cos(\varphi)}{8}\right) V_{0,\mathrm{D}}\hat{I}_1 + \left(\frac{1}{8} - \frac{M\cos(\varphi)}{3\pi}\right) R_{\mathrm{on,D}}\hat{I}_1^2. \tag{2.6}$$

where $V_{0,\mathrm{D}}$ is the threshold voltage of the diode and $R_{\mathrm{on,D}}$ is the on-state resistance [32]. The IGBT based inverter has a forward voltage drop as $V_{0,\mathrm{T}}$ and $V_{0,\mathrm{D}}$ and a resistive voltage drop as shown by the second term in (2.1) and (2.1) respectively.

2.2 Switching losses in IGBTs

When evaluating the losses of a full three-phase inverter, the switching losses also need to be taken into account. The device data sheets usually contain the necessary switching energies as a function of current levels for certain voltages and temperatures. Hence, the switching losses for one semiconductor switch can be estimated by taking every switching event into account using a look-up table approach:

$$P_{\mathrm{sw}} = \frac{\sum_{j=1}^{n=T_1 f_{\mathrm{sw}}} (E_{\mathrm{on},j} i_{\mathrm{T}}(t) + E_{\mathrm{off},j} i_{\mathrm{T}}(t) + E_{\mathrm{rr},j})}{T_1} \quad , \tag{2.7}$$

where T_1 is the fundamental period of the output voltage and E_{rr} is the reverse recovery loss of the diode. Typically the switching losses in the datasheets are measured at a certain voltage level, hence, the switching losses, $E_{\mathrm{on}}(i_{\mathrm{T}})$ and $E_{\mathrm{off}}(i_{\mathrm{T}})$, can be scaled according to the DC link voltage as

$$E_{\mathrm{on/off}}(i_{\mathrm{T}}) = \left(\frac{V_{\mathrm{DS}}}{V_{\mathrm{DC,ref}}} \right)^{K_{\mathrm{v,on/off}}} \quad . \tag{2.8}$$

The value of $K_{\mathrm{v,on/off}}$ is typically around 1.4 [33] and can be obtained from the supplier's data sheet through interpolation. Since the output current in three phase applications is normally a sinusoidal quantity, the switching loss calculation can be simplified by expressing the AC current as an equivalent DC current as

$$I_{\mathrm{DC}} = \frac{\hat{I}}{\pi} = i_{\mathrm{T}} \quad . \tag{2.9}$$

Therefore in summary, the total switching losses for one switch and the anti-parallel diode can be estimated as a sum

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} (E_{\mathrm{on}}(I_{\mathrm{DC}}) + E_{\mathrm{off}}(I_{\mathrm{DC}}) + E_{\mathrm{rr}}) \quad . \tag{2.10}$$

2.3 Losses in MOSFET based inverters

The thermal capability and the low switching losses of silicon carbide (SiC) MOSFETs can be beneficial in comparison to classical silicon (Si) IGBTs when used in a three-phase converter [34]–[37]. Available comparisons between SiC MOSFET and Si IGBT based converters show that SiC MOSFETs can achieve a more compact inverter design, while improving the system efficiency [34], [35]. Especially at high switching frequencies and high junction temperatures, the converter efficiency can be increased using SiC MOSFETs [35]–[39]. Furthermore, MOSFET based converters, as described in [40]–[44], have also reduced conduction losses at partial load operation.

In previous research [45]–[49], work has been done to derive analytical switching loss models. However, the available comparisons in [34]–[42] are mainly based on analytical conduction loss models in the literature [50]–[53] or provided by semiconductor manufacturers' application manuals [32], [54] for various IGBT and MOSFET converter topologies.

These models do not include the effect of the reverse conduction in the MOSFET inverter, also known to as third quadrant characteristic [55]–[57]. MOSFET devices typically have a body diode that allows for reverse conduction. In addition, when a negative drain-source voltage is present, the MOSFET channel's conduction can also be controlled by applying a gate-source voltage above the threshold voltage level [58]. In a three-phase inverter this results in parallel conduction of the diode and MOSFET when output voltage and current differ in sign.

The conventional way of controlling a two-level three-phase inverter is to send a PWM signal to the top switch of the inverter leg and the inverted PWM signal to the bottom one with a blanking time in between to prevent a short circuit of the leg [59]. This means that, typically, all MOSFET converters use the reverse conduction capability. Neglecting the reverse conduction can lead to overestimated conduction losses.

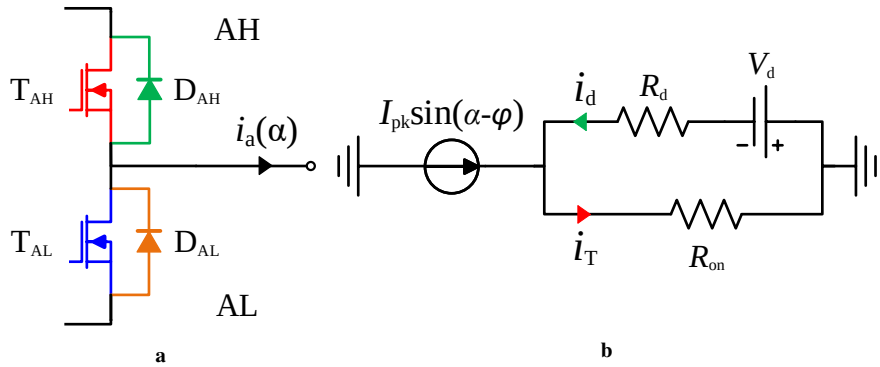


Figure 2.3: (a) Single inverter leg (half-bridge) of a three-phase inverter. (b) Equivalent circuit of parallel conduction of diode and MOSFET channel in reverse direction [58]. During the reverse conduction $i_{\mathrm{T}} < 0$, and thus the MOSFET current flows in opposite direction of the red current arrow.

Conduction losses in MOSFETs

If it is assumed that all three-phase output currents are sinusoidal and balanced it is sufficient to calculate the losses for a single inverter leg as shown in Fig. 2.3(a). Consequently, the result can be extended to the other legs. The average MOSFET conduction losses can be calculated, approximating the drain source characteristic to an on-state resistance R_{on}, as

$$P_{\mathrm{c,T}} = \frac{1}{2\pi} \int_0^{2\pi} D(\alpha) R_{\mathrm{on}} i_{\mathrm{T}}^2(\alpha) d\alpha \quad , \tag{2.11}$$

where $\alpha = \frac{2\pi}{T} t$ is the conduction angle and D is the duty cycle. Similarly, the diode conduction losses can be obtained, approximating the forward characteristic to mimic an on-state resistance R_{d} and a constant voltage drop V_{d}, as

$$P_{\mathrm{c,d}} = \frac{1}{2\pi} \int_0^{2\pi} D(\alpha)(R_{\mathrm{d}} i_{\mathrm{d}}^2(\alpha) + V_{\mathrm{d}} i_{\mathrm{d}}(\alpha)) d\alpha \quad . \tag{2.12}$$

Assuming a naturally sampled PWM sine-triangle modulation with third harmonic injection, the duty cycle can be defined as a function of α as

$$D(\alpha) = \frac{1}{2}(1 + M\sin(\alpha) + \frac{1}{6}M\sin(3\alpha)) \quad . \tag{2.13}$$

where M is the modulation index [50]. When current and voltage in one leg are of opposite signe, either the upper or the lower diode is forward biased. If the correspondent MOSFET gate-source voltage is above the threshold voltage level, the MOSFET channel conducts in parallel with the diode. Due to the constant voltage drop, the diode will only be forward biased, if the device current times the on-state resistance R_{on} is above the diode's threshold voltage V_{d} as

$$|i_{\mathrm{T}} R_{\mathrm{on}}| > V_{\mathrm{d}}. \tag{2.14}$$

This insight leads to the following cases of the MOSFET-diode conduction loss relations:

Case I - 1st quadrant operation $i_{\mathrm{DS}} \geq 0$

When the voltage and current through the MOSFET is of the same sign

$$i_{\mathrm{T}} = i_{\mathrm{DS}} \tag{2.15}$$

and the diode current is

$$i_{\mathrm{D}} = 0 \tag{2.16}$$

Thus the voltage drop across the MOSFET in the 1st quadrant operation becomes

$$v_{\mathrm{DS}} = i_{\mathrm{T}} R_{\mathrm{d}} \tag{2.17}$$

Case II - 3rd quadrant operation, no current sharing, $-\frac{V_{\mathrm{d}}}{R_{on}} \geq i_{\mathrm{DS}} < 0$

When the voltage and current are of opposite signs

$$i_{\mathrm{T}} = i_{\mathrm{DS}} \tag{2.18}$$

and the diode current is

$$i_{\mathrm{D}} = 0 \tag{2.19}$$

Thus the voltage drop across the MOSFET in the 3rd quadrant operation becomes

$$v_{\mathrm{DS}} = i_{\mathrm{T}} R_{\mathrm{d}} \tag{2.20}$$

Case III - 3rd quadrant operation with current sharing in reverse conduction, $i_{\mathrm{DS}} < -\frac{V_{\mathrm{d}}}{R_{on}}$

When the voltage and current are of opposite signs and the current magnitude is large enough so that the product from equation (2.14) is fulfilled, current sharing between the diode and the MOSFET channel occurs. This is described with the following relations for the MOSFET

$$i_{\mathrm{T}} = \frac{R_{\mathrm{on}} i_{\mathrm{DS}} - V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} \tag{2.21}$$

and the diode current is

$$i_{\mathrm{D}} = -\frac{R_{\mathrm{on}} i_{\mathrm{DS}} + V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}}. \tag{2.22}$$

where the total DS current is formed as

$$i_{\mathrm{DS}} = i_{\mathrm{T}} - i_{\mathrm{D}}. \tag{2.23}$$

As a result, the voltage drop across the MOSFET in the 3rd quadrant operation becomes

$$v_{\mathrm{DS}} = \frac{R_{\mathrm{on}} i_{\mathrm{DS}} + V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} R_{\mathrm{on}}. \tag{2.24}$$

Utilizing the results from (2.15) to (2.24) it is possible to calculate the dynamic conduction losses analytically as in

$$p_{\mathrm{c}} = v_{\mathrm{DS}} i_{\mathrm{DS}}. \tag{2.25}$$

The limits for the cases I to III are solely dependent on the device parameters, current magnitudes. Thus when calculating the average power integral for a steady state sinusioidal output current it is possible to split up the power integral limits and apply the corresponding loss formula for each of the cases.

2.4 Effect of the Blanking Time in MOSFET inverters

Because of the finite turn-on and turn-off times, associated with any type of semiconductor switch, a delay time, often referred to as blanking time, t_{bl}, between the conduction of the upper and lower switch of the same inverter leg must be imple-

Figure 2.4: Effect of the blanking time on the diode and MOSFET current.

mented in order to avoid a shoot-through. During the blanking time only the diode is conducting the current. In the case of the IGBT inverter when the inverter through the switch is negative it always goes through the anti-parallel diode, unlike the MOSFET which conducts in the reverse direction. Therefore, this effect is only considered for the MOSFET inverter. As a result, the effect of the blanking time is shown in Fig. 2.4. Its effect on the MOSFET conduction loss calculation can be accounted for by defining an equivalent duty cycle as

$$D_{\mathrm{eq}}(\alpha) = \mathrm{D}(\alpha) - t_{\mathrm{bl}} f_{\mathrm{sw}} = \frac{1}{2}(1 - 2t_{\mathrm{bl}} f_{\mathrm{sw}} + M\sin(\alpha)) \ , \tag{2.26}$$

where t_{bl} is the blanking time and f_{sw} is the switching frequency. Negative duty cycle values are not to be considered, so the condition

$$1 - 2t_{\mathrm{bl}} f_{\mathrm{sw}} + M\sin(\alpha) > 0 \tag{2.27}$$

must be verified in the case of a sinusoidal reference voltage. Normally a third harmonic component injection is

$$1 - 2t_{\mathrm{bl}} f_{\mathrm{sw}} + M\sin(\alpha) + 1/6M\sin(3\alpha) > 0 \quad . \tag{2.28}$$

For values of M close to the boundary of the over-modulation region, the method of using an equivalent duty cycle should be applied carefully. Typically a third harmonic component of $1/6$-th of the fundamental is added. Negative duty cycle values are to be avoided. Since the diode is conducting the whole current during the blanking time, the average conduction losses of the diode must be extended by the addition of

$$\frac{1}{2\pi} \int_{\pi}^{2\pi} 2t_{\mathrm{bl}} f_{\mathrm{sw}} \left(R_{\mathrm{d}} \hat{I}^2 \sin^2(\vartheta) - \hat{I}\sin(\vartheta) V_{\mathrm{d}} \right) d\vartheta \quad , \tag{2.29}$$

which results in

$$t_{\mathrm{bl}} f_{\mathrm{sw}} \hat{I} \left(\frac{1}{2} \hat{I} R_{\mathrm{d}} + \frac{2}{\pi} V_{\mathrm{d}} \right) \quad . \tag{2.30}$$

While the MOSFET and diode conduction losses have been derived without introducing any approximation, the formulas including the blanking time have some degree of

approximation. Using an equivalent duty cycle as in (2.26) means a reduction of the current conduction interval with two times the blanking time. However, the blanking time intervals are not specifically placed at the beginning or the end of the reverse conduction, but are considered averaged over the whole electrical period, introducing a small error.

Switching Losses in MOSFETs

Switching losses in MOSFETs do not differ from those discussed in the IGBT chapter in any significant manner. Having the MOSFET turning on and off during reverse conduction would in theory increase the switching losses. However, due to the fact that the diode is conducting in parallel or is conducting during the blanking time, the voltage across the MOSFET is forced to $V_{\mathrm{d}} + R_{\mathrm{d}}\hat{I}$ during the beginning of the switching transient, achieving quasi zero-voltage-switching (ZVS). Therefore, the switching losses of the MOSFET during reverse conduction are negligible.

2.5 Experimental verification of the MOSFET loss model

In this section the process of the experimental validation of the proposed model is described in detail. First the experimental setup is described, then the calibration of the loss measurement is discussed and finally the measurement results are discussed and compared to the modelled losses.

The experimental setup

For the validation of the conduction loss models described in the previous section, a SiC MOSFET based 2L-VSI is prototyped utilizing a Cree power module in a six-pack configuration. An evaluation gate driver board from Cree is used to drive the switches. The bill of materials used in the inverter and the sensors are shown in Table 2.1.

The double jacketed calorimetric box, as described in [62], has an inner and an outer air chamber. Having two chambers reduces the leakage heat through the box walls. The inverter and heatsink are fitted inside the calorimetric box with high resolution 4-wire PT100 temperature sensors at the water inlet and outlet of the inner box.

Table 2.1: Equipment list

Device	Manufacturer	Model
SiC module 1.2 kV/50 A	Wolfspeed	CCS050M12CM2[60]
SiC gate driver board	Wolfspeed	CGD15FB45P1[61]
2 DC link capacitors 5 µF	Vishay	MKP386M550125YT4
4W-PT100	RS PRO	25mm x 4mm Probe
Acquisition unit	Fluke	Hydra 2620A
Pump	Shenchen	LabN6

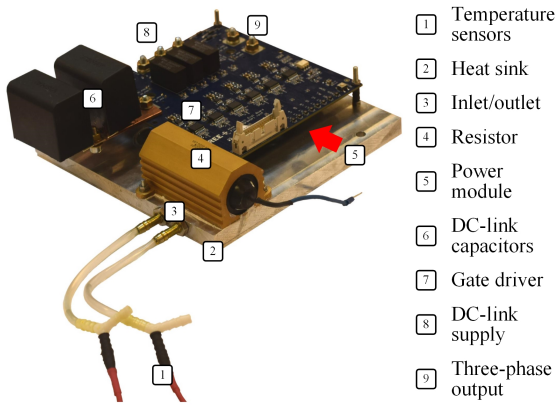


Figure 2.5: Three-phase inverter prototype and calibration resistor mounted on the water cooled heatsink.

The inverter inside the box is equipped with a 220 Ω calibration resistor with a maximum power dissipation of 100 W and is mounted on the water cooled cold plate as shown in Fig. 2.5. The role of the calibration resistor is to inject a well defined DC voltage and current creating a loss in the inverter system. By comparing the injected DC power into the inverter system with the measured extracted heat energy from the cooling circuit a leakage factor σ_{th} can be established.

The selected coolant pump is a medical grade pump able to operate with a high accuracy at very low flow rates. A low flow rate of $200\,\mathrm{mL\,min^{-1}}$ is selected in

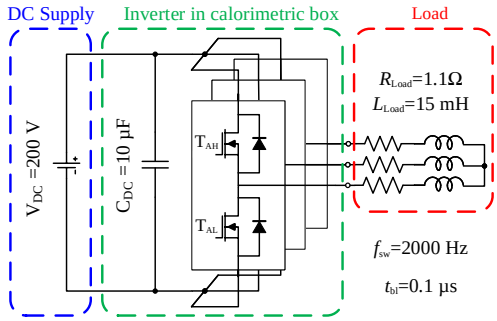


Figure 2.6: Schematic operation of the inverter setup, using an RL-load. The low switching frequency and the low DC-link voltages reduce the switching losses.

order to increase the outlet to inlet water temperature delta and hence the accuracy of the measurement. When measuring losses in the range of 10-30 W this becomes a necessity. The coolant medium is tap water kept in a large reservoir.

The PWM signals are generated using a dSpace DS1006 processor board and DS5202 FPGA Base Board. A program is implemented to be able to enable the reverse conduction, W-RC, and disable the reverse conduction, W-RC, by either providing a high or a low gate signal to the corresponding SiC MOSFET when voltage and current are of opposite sign. A schematic description of the program is presented in Fig. 2.7. The fundamental logic is to compare the phase current to a threshold current level which is close to zero. For example, if W-RC is enabled, then the top switch of phase a is kept off during the negative half cycle of the fundamental period. If W-RC is enabled then the top and bottom switch gate signals are inverted to each other.

The switching frequency of 2 kHz is selected and the DC-link voltage is chosen to be 200 V. These values are selected in order to minimize the impact of the switching losses on the total measured loss. The load is an RL-load. The electrical schematic of the system can be seen in Fig. 2.6 Different power factor operating points are investigated by changing the fundamental frequency. To ensure that the current amplitude remains the same, a current controller is implemented.

The complete laboratory setup is shown in Fig. 2.8.

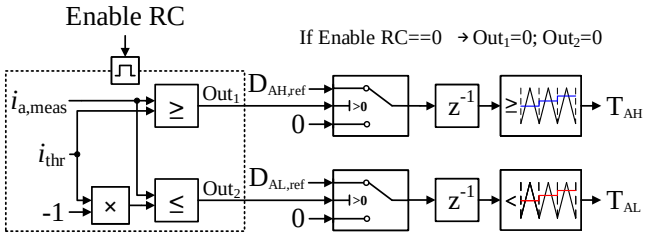


Figure 2.7: Schematic description to disable the reverse conduction by keeping the gate switched off, if the phase current exceeds the threshold value i_{thr}.

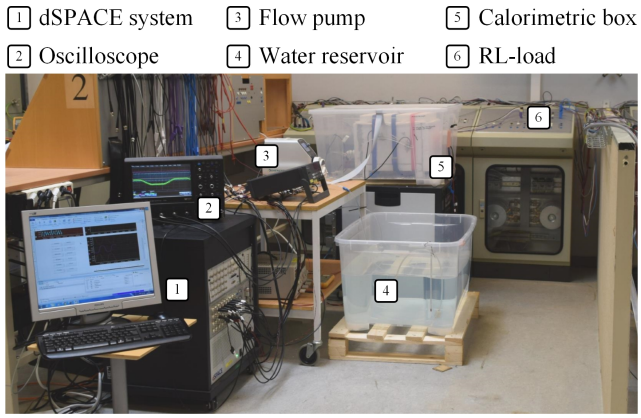


Figure 2.8: Actual test setup environment with calorimetric box, water reservoir, data acquisition and control unit.

Calibration of the measurement

The MOSFET on-characteristic and diodes voltage drop are measured at room temperature. Additionally, the reverse conduction effect of the third quadrant is recorded at different drain-source current levels. This measurement is done in order to verify the stated datesheet values. The results in comparison to datasheet values are shown in Fig. 2.9.

Estimation of the thermal leakage factor σ_{th} of the calorimetric system is done by applying a DC voltage step to the resistor for an estimated loss injection of approximately 25 W. Figure 2.10 shows the thermal response of the system where inlet and outlet water temperatures as well as the internal ambient temperature are measured.

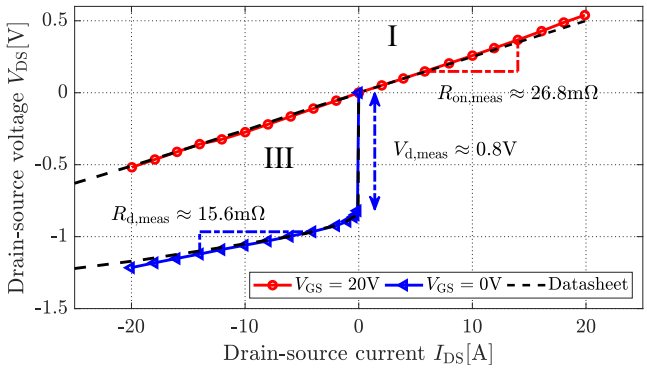


Figure 2.9: Measured MOSFET and diode characteristic of the chosen SiC MOSFET inverter. Reverse conduction is also shown.

After an initial rise, the absolute temperatures inside the box can be seen rising at a constant rate. This is because the outlet water is disposed into a water reservoir which slowly heats up. This reservoir has at the other far end the intake to the coolant inlet. As a result, over time, a slow warming of total system can be observed. The coolant outlet to inlet temperature delta however remains constant after the first transient. This is found to be a quasi steady state for the loss evaluation.

The calibration procedure is done for several different levels of injected power. The leakage factor is found to be relatively constant within the measured power range as can be seen in Fig. 2.11. An average value is therefore used when estimating losses of the inverter in the subsequent measurements.

Finally the inverter losses can be estimated by

$$P_{\text{loss}}(1 - \sigma_{\text{th}}) = c_{\text{p}} \dot{V} \rho \Delta T \quad , \tag{2.31}$$

where σ_{th} is the calorimetric box's leakage factor, c_{p} is the heat capacity at constant pressure, $\dot{V}$ is the volumetric flow rate, ρ is the volumetric mass density and ΔT is the temperature difference between the inlet and the outlet.

Loss measurement results of the MOSFET inverter

The inverter's output current is at first controlled to 20 A peak at a fundamental frequency of 50 Hz. The high and low side gate signals together with the output current and the voltage reference of the measurements for one of the three phases are shown

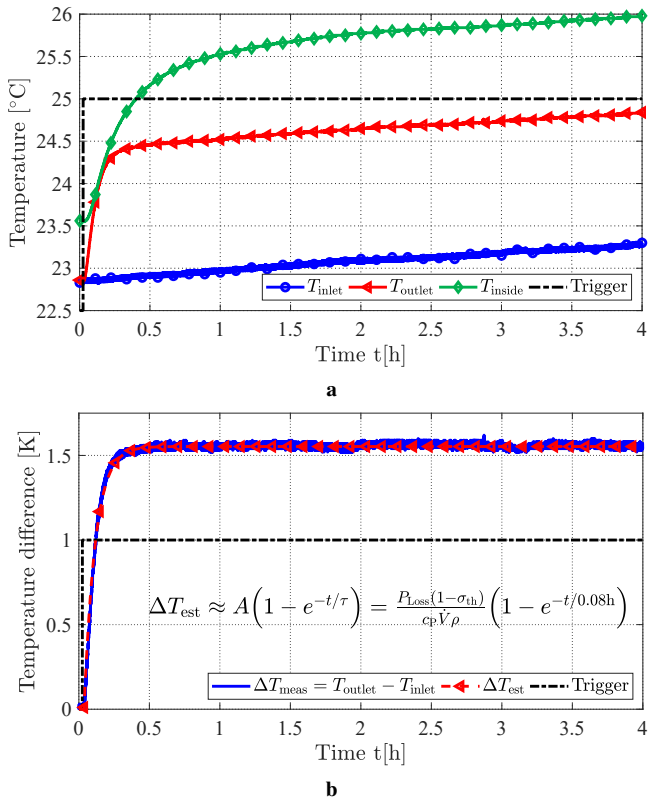


Figure 2.10: Transient temperature profiles using a flow rate of $200\,\text{mL}\,\text{min}^{-1}$ for about $25\,\text{W}$ of injected power. (a) Temperature profiles of the water inlet, water outlet and the air inside the box. (b) Water temperature difference between the outlet and the inlet, both measured and estimated.

in Fig. 2.12 for the W-RC case. It can be seen that when operating in W-RC mode the gate signals to top and bottom switch are complimentary. The resulting output current is also depicted. The corresponding voltage reference is obtained from the dSpace signal interface.

In Fig. 2.13 a similar measurement is performed for the WO-RC case. It can be observed that when the current is of positive sign, the bottom switch is not being activated and only the top switch is performing switching actions. The case is opposite when the current is of negative sign.

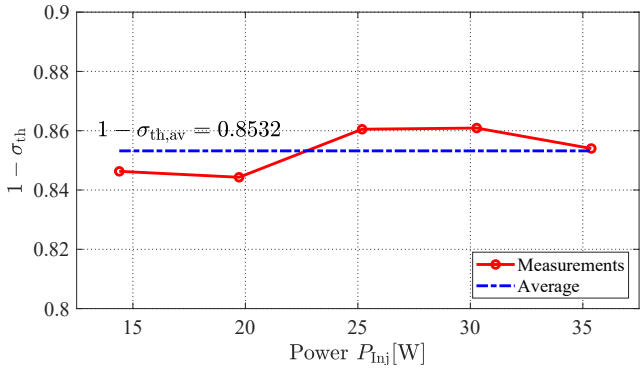


Figure 2.11: Calorimetric box's leakage factor measured for different power levels of injected DC power using the calibration resistor.

The associated temperature difference between the outlet and inlet of the calorimetric setup can seen in Fig. 2.14. The inverter was operated in intervals of approximately $1\,\mathrm{h}$ in with and without reverse conduction modes. The effect of the reverse conduction has a significant impact on the inverter losses. When the inverter is operated in W-RC mode the reverse conduction is in effect and the temperature delta is approximately $1.2\,\mathrm{K}$. When operated in W-RC mode the current is forced through the diode which results in a larger loss and as a result a larger temperature increase of the coolant - approximately $1.7\,\mathrm{K}$.

The WO-RC mode of operation is actually akin to the principle operation of an IGBT based inverter where no reverse conduction is possible.

The total measured loss includes auxiliary losses such as caused by he gate driver board inside the calorimetric box. Typically, gate driver losses can be discounted when designing inverters, however in these high precision measurement at low loss levels this is necessary. The measured auxiliary losses from the gate driver board amount to $(2.8\,\mathrm{W})$. In theory the gate driving loss is also dependent on the switching frequency, however when the datasheet of the gate driver is studied it is found that this dependency amounts to $\Delta P_{\mathrm{Aux}} \approx 33\,\mu\mathrm{W\,Hz^{-1}}$ [61]. As a result the difference of the effective gate driver switching frequency between the cases W-RC and WO-RC was $1\,\mathrm{kHz}$, which should result in a theoretical auxiliary loss difference of about $33\,\mathrm{mW}$. In practice however this difference in is not observable in the measured auxiliary power consumption.

The switching losses are quantified by applying (2.10) and result in approximately

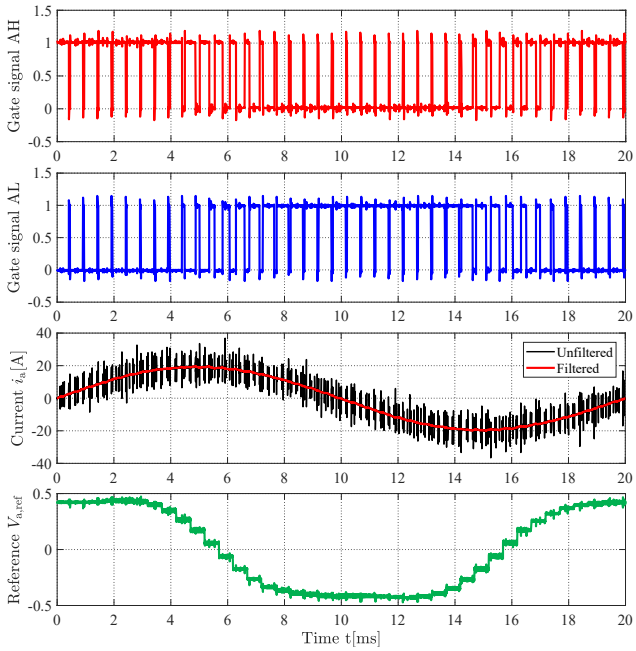


Figure 2.12: Gate signals, reference voltage and output current with enabled reverse conduction (W-RC) for one of the three phases.

0.2 W, for both W-RC and W-RC. Finally when estimating the total inverter losses the switching and the auxiliary losses are added to the conduction losses calculated with the analytical model and compared with the total losses measured in the calorimetric setup. The results show very good agreement as can be seen in Fig. 2.15 where the calculated and measured conduction loss separation is performed for both cases. When the case with W-RC is investigated, the presented analytical expressions show an agreement of approximately 98.5 % compared to the measured losses.

The above described procedure is repeated for several different operating points in terms of current amplitude and power factors by varying the fundamental frequency. The final results are shown in Fig. 2.16. The results show, as predicted, that for a MOSFET based inverter the losses are not significantly dependent on the output power factor or modulation index. The total loss is mainly dependent on the current amplitude. The measured losses match very well with the ones predicted using the analytical model across all investigated operating points.

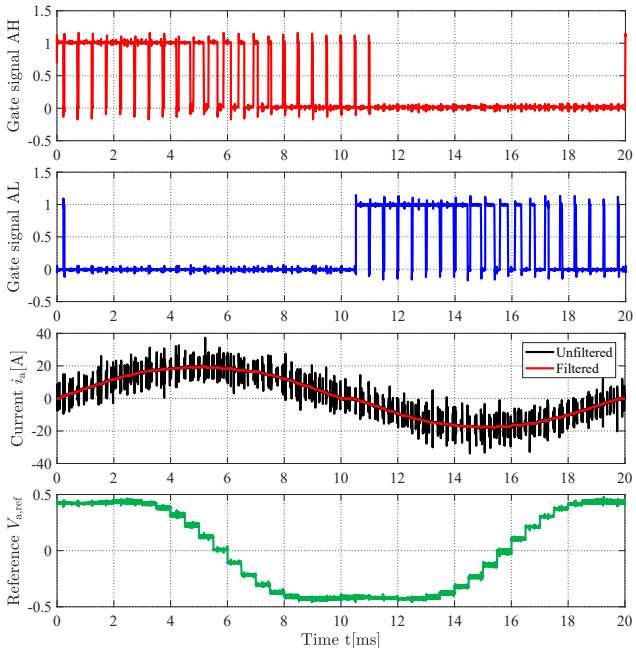


Figure 2.13: Gate signals, reference voltage and output current with disabled reverse (WO-RC) conduction for one of the three phases.

Comparison of the two compared methods when estimating losses

The MOSFET-based inverter features the reverse conduction characteristic. Therefore especially during partial load where compared to the IGBT based inverter the MOSFET based inverter does not feature a diode like forward voltage drop. Therefore especially during partial load loss estimation the method discussed in section 2.1 will lead to significant errors. Furthermore, the suggested method also takes into account the effect of parallel conduction of the MOSFET and the diode making it accurate in the high current operating points too. A comparison between the estimated loss using the method using the method W-RC and W-RC is made in Fig. 2.17. It can be seen that particularly at partial load operation with low power factor the error in using the traditional method, [32], yields large errors.

In conclusion - neglecting the reverse conduction can lead to errors in the conduc-

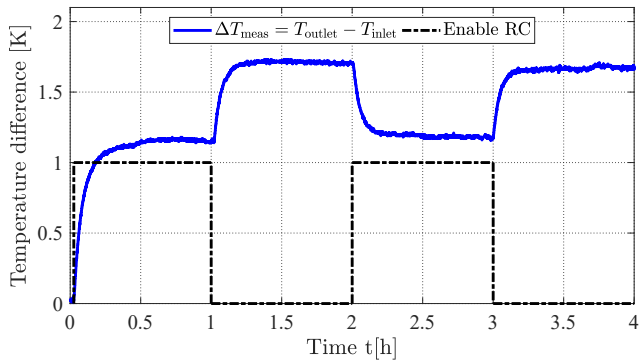


Figure 2.14: Measured water temperature difference between the outlet and the inlet with alternately enabled and disabled reverse conduction for a current amplitude of 20 A at 50 Hz.

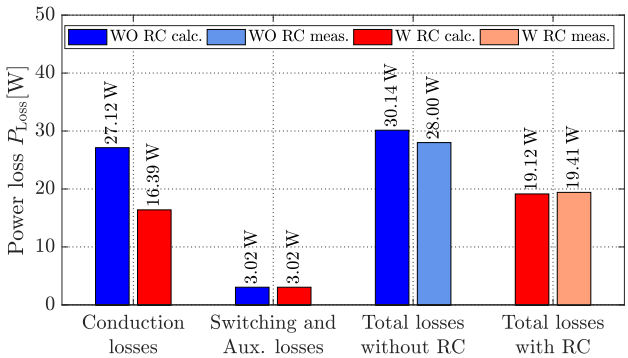


Figure 2.15: Comparison of estimated losses, using the analytical models, and measured losses for a current amplitude of 20 A at 50 Hz.

tion loss estimation, which could result in an overdimensioned cooling system when utilizing MOSFET-based inverters.

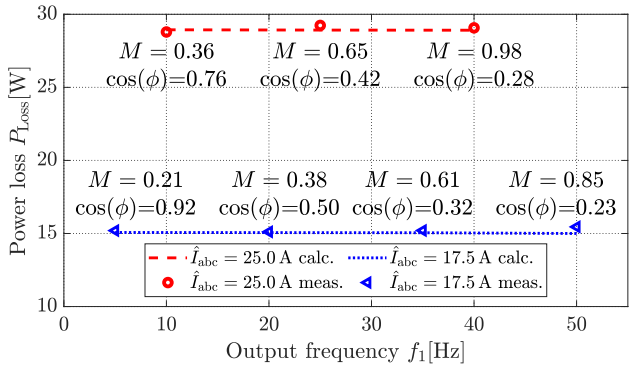


Figure 2.16: Comparison of estimated losses, using the analytical model, and measured losses for different operating points with enabled reverse conduction.

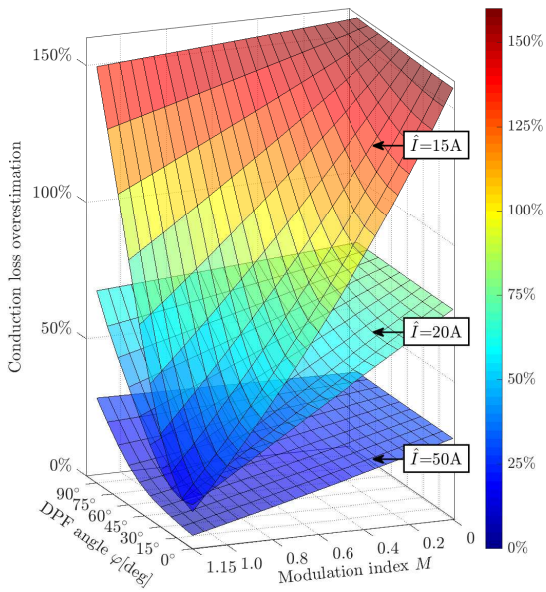


Figure 2.17: Overestimation of the conduction losses when using the method that does not take into account the reverse conduction effect in comparison to the presented method for the SiC MOSFET three-phase inverter of Cree

2.6 Temperature dependence of MOSFET loss parameters

One of the limiting factors when conducting the calorimetric measurement was the current limit of the load which was rated at $18\,\mathrm{A}$ RMS ($25\,\mathrm{A}$ peak). Therefore the rated current of the power module was not reached. The derived expressions in previous sections can further be expanded with temperature dependent variables. Typical parameters whose parameters temperature dependence influences losses are the on resistance, R_{on}, switching energies $E_{\mathrm{on/off/rec}}$ and the threshold voltage of the diode V_{d}. Typically these temperature dependencies are available in datasheets [60]. It is therefore possible to implement these temperature dependencies using look up tables.

A traction application is selected to perform this study where a PMSM electric machine is selected and its key parameters are shown in Table 2.2. An electric vehicle application is interesting for this study as it offers partial load as well as full load operating points to study from an inverter point of view. The selected machine is developed for $400\,\mathrm{V}$ DC link and delivers a peak torque of $197\,\mathrm{Nm}$ and has a maximum speed of $9000\,\mathrm{rpm}$. A typical requirement for vehicle applications is that the components must deliver rated power at a coolant temperature of $65\,^{\circ}\mathrm{C}$.

In order to implement a thermally dependent model one needs to consider the thermal network of the power semiconductor structure in a finalized system including heatsink and thermal interface materials. Typically this type of work requires a large engineering effort and needs to be made in an iterative fashion with loss estimation and cooling performance of the cooling system. A simplified approach with an equivalent thermal resistance of $0.5\,\mathrm{K/W/switch}$ is chosen to investigate the temperature dependence of losses. Thermal capacitances are neglected because in power electronic inverters the thermal constants are typically $\leq 1\,\mathrm{s}$ and therefore the steady state operating point is reached relatively quickly from the inverter point of view. The thermal boundary conditions for the system are the coolant temperature and the junction temperature of the switch, $T_{\mathrm{j,max}}$. The thermal network for a SiC MOSFET based inverter without an external anti-parallel Schottky diode is shown in Fig. 2.18. Here the switch is acts as a power source and has a temperature. The thermal resistances consisting of the chip's own thermal stack R_{jc} and the heatsink thermal resistance R_{jc} shown schematically between the chip and coolant.

The inverter is comprised off a $1.2\,\mathrm{kV}/100\,\mathrm{A}$ SiC-MOSFET from Cree/Wolfspeed [63]. To achieve the necessary current rating each switch position contains 4 parallel MOSFETs. The inverter system in the simulation is summarized in Table 2.3.

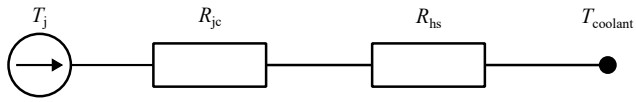


Figure 2.18: The simplified thermal network from junction to coolant.

Table 2.2: Permanent magnet motor parameters in the simulation

Parameter	Value	Unit
DC link voltage V_{dc}	400	V
Stator resistance R_{s}	26	mΩ
d-axis inductance, L_{d}	0.45	mH
q-axis inductance, L_{q}	1.30	mH
Pole pairs , n_{p}	4	–
Peak torque, T_{max}	197	Nm
Peak phase current, $\hat{I}$	320	A
Max speed, n	9000	rpm

The above mentioned inverter and machine are modelled in Matlab/PLECS. The loss calculation of the inverter is performed by a number of 3D-loss maps in accordance to the motor operating points. Each operating point inside the torque and power boundaries the corresponding d and q axis currents are calculated according to the governing equations of the PMSM. MTPA and field weakening is respected with regards to the current and voltage constraints of the system. Thus, a PI-regulator is utilized in the control of the motor currents for fixed motor speed operating points. The operating points in terms of current magnitude, modulation index, power factor and other relevant factors are recorded for later comparison with the analytic model. The losses at each operating point are recorded from the pre-calculated lookup tables based on the thermal model provided by the manufacturer [63].

For the comparison between the analytical formula NTF and WTF a recursive function is built with a convergence criteria of $0.1\,^{\circ}\mathrm{C}$. The fundamental idea is to calculate the junction temperature based on the losses and thermal resistance network. Thermal capacitances are neglected and are assumed to have a total time constant of less

Table 2.3: Key inverter parameters in the simulation. The superscript ^{1} denotes nominal values of the switch at $25\,^\circ\mathrm{C}$ [63]

Parameter	Value	Unit
Switching frequency, f_{sw}	20	kHz
Blanking time, t_{bl}	140	ns
On resistance, R^1_{on}	21	mΩ
Diode resistance, R^1_{d}	23	mΩ
Diode threshold voltage, V^1_{d}	2.78	V
Thermal resistance, R_{th}	0.5	K/W/MOSFET
Coolant temperature, T_{coolant}	65	°C

than $1\,\mathrm{s}$ and hence to be suitable for most drive cycle studies. The junction temperature, T_{j}, is then updated based on this loss and compared to the previous value. If the convergence criteria is not met the loss calculation is performed recursively until a steady state final loss temperature is found. The loss value is then recorded. This process is described in Fig. 2.19

The results of the NTF and WTF models as well as the thermally coupled PLECS simulation are shown in Figs. 2.20a, 2.20b and 2.20c respectively. The PLECS simulation is then taken as a reference and the relative error between the PLECS simulation and the analytical methods is shown in Figs. 2.21a and 2.21b. It can be seen that at peak torque the NTF model underestimates the conduction loss up to $30\,\%$ compared to the PLECS simulation. On the other hand the WTF model is for most high current operating points within $5\,\%$ of the reference PLECS simulation. The largest deviation of the WTF model is observed at low speed high torque where the model overshoots by approximately $10\,\%$. This however could be due to poor performance of the implemented controller at low speed / high torque operating points.

The improvement by including the thermal effect to the loss calculation is relatively low effort and yields very accurate results in relation to the numerical simulation. The benefit in this improved method apart from the accuracy is the speed when using the analytical function. The analytic model takes a few seconds to compute the complete presented loss map on a normal desktop computer whereas the PLECS loss map takes roughly $12\,\mathrm{h}$ to obtain. The computer used in the simulation has an Intel i7-7700 CPU

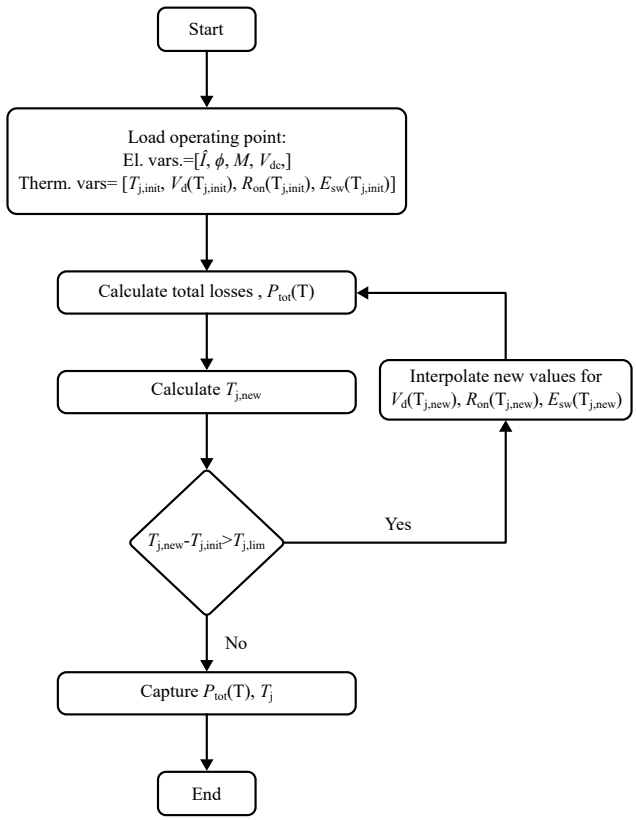


Figure 2.19: Recursive algorithm for analytic loss loss calculation with thermal feedback

operating at 3.60GHz (8 CPUs). As a result, the suggested improved analytic model (WTF) makes a very convenient tool with high accuracy when iterating the switch selection for an inverter prototype.

Summary of MOSFET loss modelling

In summary analytical models to quickly evaluate the conduction losses of a three-phase inverter are discussed. The MOSFET model includes the effect of the reverse parallel conduction and blanking time. These models can be used as a quick and accurate tool during the inverter design process to evaluate the inverter efficiency and to perform thermal evaluations as well as drive cycle stuidies.

The proposed equations for MOSFET losses have been experimentally validated. A SiC MOSFET inverter was tested at different operating points and the losses were measured using a calorimetric setup. The measured losses were compared with the proposed analytical models with good agreement. Further, the analytic model has then been expanded to include look-up tables of temperature dependent losses for the switching energies and on state resistance as well as diode reverse conduction threshold voltages. The presented method is compared to numerical simulations and the agreement is good across the whole operating map of a PMSM for traction vehicle application.

In comparison to the presented method with other available methods for IGBT inverters it is clear that neglecting parallel reverse conduction will overestimate the conduction losses when applied used to MOSFET inverters, especially at partial load operation when the diode might not reach its threshold voltage. On the other hand not including the thermal effects on the losses could lead to significant under-estimation of losses in high load operating points, which could cause overheating if the cooling system is underdimensioned.

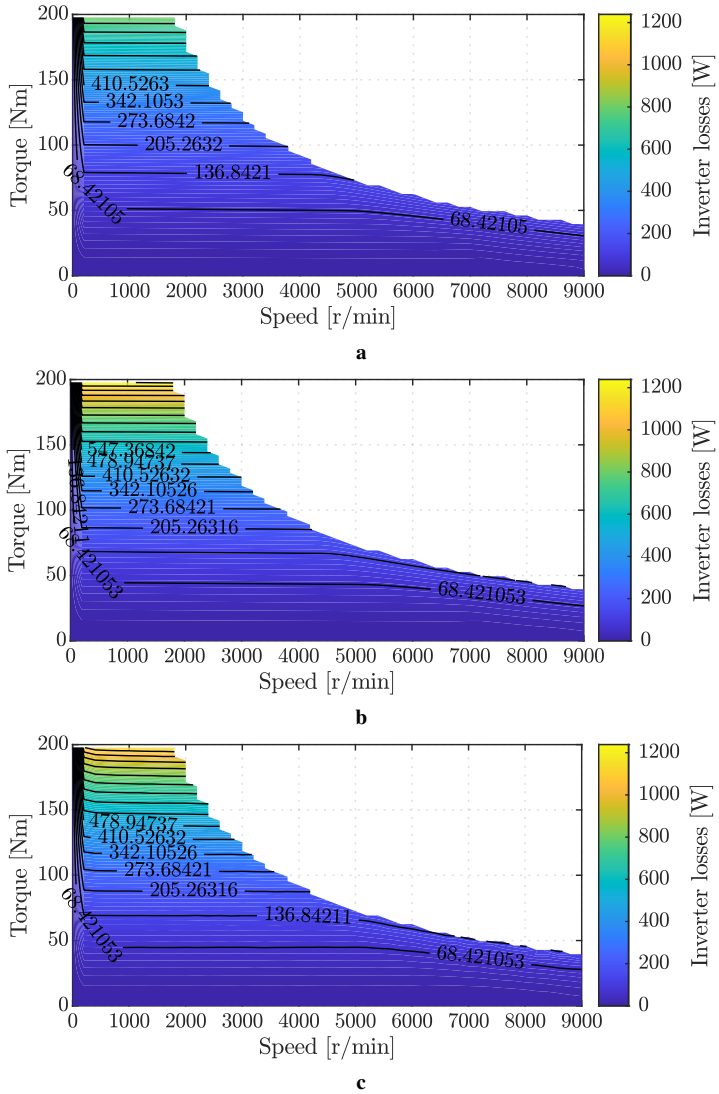


Figure 2.20: Total conduction loss results (a) without thermal feedback, (b) with thermal feedback and (c) PLECS numerical result.

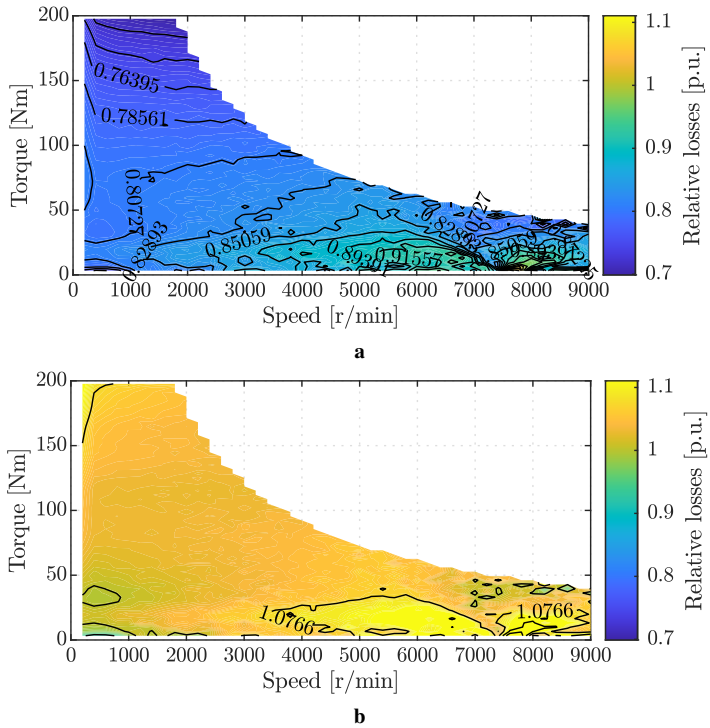


Figure 2.21: Comparison of conduction loss models relative to the simulated PLECS result (a) without thermal feedback effect, (b) with thermal feedback effect.

CHAPTER 3

Capacitors in electric vehicles

This chapter will explore the functionality, limitations and dimensioning of capacitors and provide an overview of their use in DC-link applications for inverter and electric vehicle applications. A numerical method is developed for estimating the current and voltage stress in a two level VSI. This method is expanded to estimate the current stress in a DTP application with carrier wave interleaving as a way to reduce the capacitor bank stress. Guidelines for capacitor current and voltage stress optimization are developed on the basis of this method.

3.1 Introduction

Inverter and electric vehicle applications require the conversion of DC power to AC power, which involves the use of power electronic switches that rapidly switch on and off [24]. These switches generate high-frequency voltage ripple in the DC-link circuit that can cause problems such as electromagnetic interference, reduced efficiency, and voltage instability. DC link capacitors are essential components in these circuits that are used to mitigate these problems by smoothing out the voltage ripple and maintaining a stable DC voltage supply to the inverter's switches [24], [64], [65].

In the traditional three phase inverter the DC link capacitor has a large space claim,

up to $50\,\%$, especially if electrolytic capacitors are used [23]. The space claim of capacitors in inverter applications is an important design consideration that can impact the overall size and weight of the system. In general, the amount of space required for capacitors in an inverter circuit is determined by the required energy storage capacity and the operating voltage. Therefore, optimizing the capacitor bank sizing is of premier importance for high power density drives.

The DC link stress for three phase inverters has been studied in numerous previous publications [24], [64], [65]. These studies provide analytical methods to calculate the RMS current stress on DC link capacitors in PWM moulated converter systems. The derived equations to calculate the RMS current stress includes the system parameters such as switching frequency, load current, and DC-link voltage. The results include that the capacitor size increases with increasing RMS current stress and decreasing switching frequency.

In recent years the multi-three-phase inverter based systems, depicted in Fig. 3.1, connected to multi-three-phase machines have gained popularity [25], [66], [67]. Fig.3.1 shows that on the output side, the multi-three-phase inverters consist a multiple parallel connected three phase bridges. Whereas the input DC side is still only two terminals and a shared DC link capacitor bank between all the outputs. When designing a multi-three-phase inverter, the total output power is the same. However, because the amount of phases increases, the output current is scaled according to

$$I_{\mathrm{n\times 3ph}} = \frac{1}{n} I_{\mathrm{3ph}}, \tag{3.1}$$

where n is the multiple of number of three-phase systems. Hence, the total needed semiconductor area stays approximately the same in both 3-phase and for example - 6-phase cases.

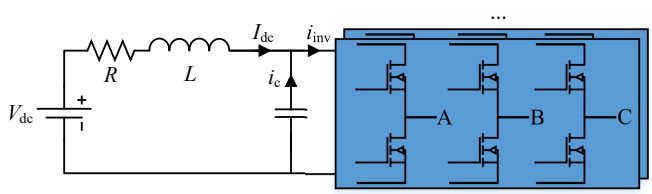


Figure 3.1: Multi-phase inverter with common DC link.

It has been reported that the multi-three-phase topology offers benefits in terms of reduced DC link capacitor current stress [26], [68]–[70]. Hence the multi-phase

design can be used to improve the power density of the inverter and the system. Capacitor sizing for multi-phase applications has been studied for in [26], [71]. However, in those works no thorough investigation of power factor is present. Furthermore in most capacitor sizing and dimensioning papers the DC link voltage ripple is not studied. This requirement is important since excessive DC link voltage ripple emitted by the propulsion motor system can damage auxiliary equipment connected to the traction battery.

DC link capacitors are characterized by the technology that is utilized in the construction like has been mentioned in Chapter 1.1. The fundamental working principle of a generic capacitor is a parallel plate capacitor with two terminals and a dielectric material. The capacitance of a a parallel plate capacitor can be expressed as

$$C = \frac{\varepsilon A}{d} \tag{3.2}$$

where C denotes the capacitance, ε the dielectric permittivity of the material, A is the area of the plate and d is the distance between the plates. As can be seen the capacitance depends on the the permittivity of the dielectric material, area of the plates (size) of the capacitor and the distance between the electrode plates. The minimum value of thickness is limited by the required dielectric strength for the necessary operating voltage. Therefore, d, and hence the capacitance, is inversely proportional to the operating voltage of the capacitor for the same dielectric [31].

Aluminium electrolytic capacitors are commonly used in drive applications [23]. The benefits of electrolytic capacitors include high capacitance values (CV-values) and relatively low current rating, low temperature application. The dielectric typically consists of aluminium oxide, $\mathrm{Al_2O_3}$, which can feature low value of d and hence increase the capacitance of the product. On the other hand however, the $\mathrm{Al_2O_3}$ layer is liquid. and calendar ageing effects due to the evaporation of the chemicals in the dielectric [72]. This evaporation may lead to catastrophic failure of the equipment if the decaying capabilities are not accounted for in the design stage. Typical construction and packaging of an electrolytic capacitor is rolled electrolytic material in a sandwich configuration between the cathode and anode foil. The large characteristic C rating of this type of capacitors makes them suitable for switching applications that require a very low degree of voltage ripple and/or low switching frequency applications [65].

Film capacitors made of metallized film consist of two plastic film pieces coated with metallic electrodes that are wound into a cylindrical shape and enclosed with attached terminals. Typically, film capacitors are non-polarized, which means the

two terminals can be interchanged. Film capacitors are today commonly employed in traction applications as they offer higher current rating capacity then their electrolytic counterpart [65]. Compared to electrolytics they also feature lower CV values, but due to the relatively high switching frequency ($>10\,\mathrm{kHz}$) in today's electric vehicles this is not considered a problem and most often the current carrying rating of the film capacitor is the sizing criteria [65]. Due to the solid nature of the dielectric, the there is no evaporating ageing effect in film capacitors which improves their ageing characteristics [31]. Due to this, film capacitors feature higher operation temperatures than electrolytes. The electrode of the metallized film capacitors can be subdivided into elementary cells with fuse gates. In the case of a dielectric puncture, only the fuses will be burnt and the bulk capacitor still remains functional at a reduced rate. This is commonly referred to as self healing characteristics which improve safety greatly [73].

Lastly ceramic capacitors are constructed by sandwiching a ceramic dielectric material between two conductive plates, which are then coated with a protective layer. They are small in size, offer high capacitance values, and can operate at high frequencies, making them suitable for use in a wide range of electronic applications. However, they have a tendency to exhibit nonlinear capacitance behavior, and their capacitance values can be sensitive to temperature and voltage changes. Furthermore, ceramic capacitors may experience a phenomenon known as the piezoelectric effect, which can result in electrical noise and distortion. Despite these drawbacks, ceramic capacitors remain popular due to their low cost, high reliability, and compatibility with surface-mount technology. At DC link voltage levels typical for EVs, such as $400\,\mathrm{V}$ to $800\,\mathrm{V}$ the ceramic capacitors have a rather low C-rate would lead to large voltage ripples [74]. Due to their high current carrying capability and low capacitance the design point for ceramic based capacitor bank could be the capacitance value and not the ripple current. With new wide bandgap devices such as SiC and GaN which feature improved efficiency and switching frequency [75], it could be possible to utilize ceramic capacitors.

3.2 Ideal DC link modelling

In this section a reference permanent magnet synchronous machine is defined and briefly introduced. The various possible winding connection configurations and their impact on the DC link modelling are discussed. Based on these configurations a DC link modelling case is presented and employed. The various effects of winding

connection configuration, modulation and operating points are studied and discussed.

The electric machine and winding configurations

The selected machine for the case study is the 12 slot 10 pole fractional slot (FSCW) machine. It is considered as an attractive solution for automotive electrification due to high fundamental winding factor, short end-windings and ease of mass production [76]–[78]. Furthermore, this machine is selected as it is possible to configure it in 3-phase mode and in 6-phase mode. The 6-phase mode offers some benefits in terms of redundancy but also in somewhat higher torque which are attractive features in automotive applications [78], [79].

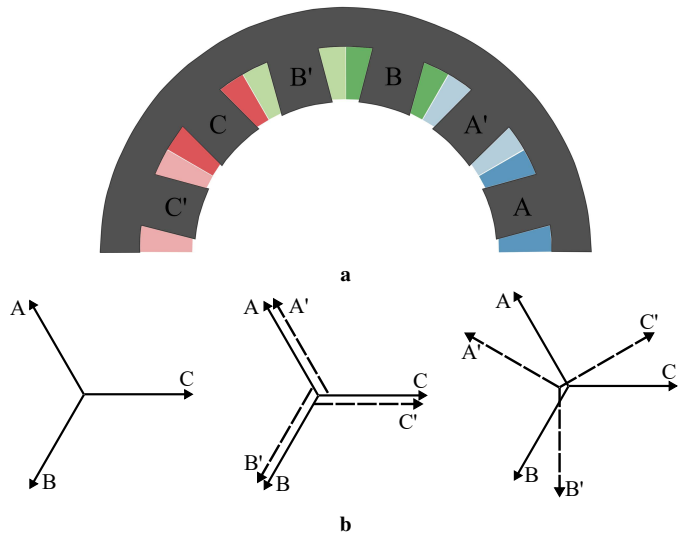


Figure 3.2: (a) 12 slot 10 pole machine disposition, (b) phasors for *Case 1*, *Case 2* and *Case 3* respectively

The machine under consideration is shown in Fig. 3.2a. It is an interior v-shape magnet PMSM with concentrated windings. Here, the impact of winding configurations and PWM carrier wave interleaving and their effects on the DC link sizing is studied. The winding of this machine can be connected either in 3-phase mode or 6-phase mode. The possible cases as shown in Fig. 3.2b are:

Case 1

3-phase mode supplied by one 3-phase inverter where the coils A and A' are connected in series. The corresponding coils on the other side of the stator are connected in series as well to form two branches of phase A.

Case 2

Pseudo 6-phase mode where coil A and A' are supplied by two parallel 3-phase inverter bridges with zero phase shift between phases. Each star system has its own PWM carrier. The neutral points are isolated.

Case 3

6-phase mode with $30\,^\circ$ phase shift between the stars and supplied by two parallel 3-phase inverter bridges and the neutral points are isolated. Similarly to *Case 2* each star system is supplied with its individual PWM carrier.

By sweeping the different offsets between the PWM carrier waves it is possible to find the optimum shift which results in the lowest possible capacitor current or voltage stress. The benefit of *Case 2* compared to *Case 1* is that this case has redundancy which is possible to utilize in safety critical applications. Furthermore, in *Case 2* the control is simpler than in *Case 3*. On the other hand, *Case 3* allows better utilization of the DC link voltage due to improved the winding factor k_{w} [79]. The resulting current vectors for the cases are shown in Fig. 3.2b. The PWM interleaving is visualized in Fig. 3.3 [25], [26].

Capacitor current modelling

The switching actions in the a an inverter are controlled by comparing the reference voltage with a triangular carrier. The reference voltage signal is

$$v_{\mathrm{ref}}(t) = M\sin(\omega t + (n-1)\varepsilon), n = 1, 2, 3, .., N \tag{3.3}$$

where M is the amplitude modulation index and ε is angle between phases based on winding configuration and N is the total amount of phases.

In modern drive systems a zero sequence component is added to the fundamental wave. This component increases the operating voltage window. In sine wave PWM

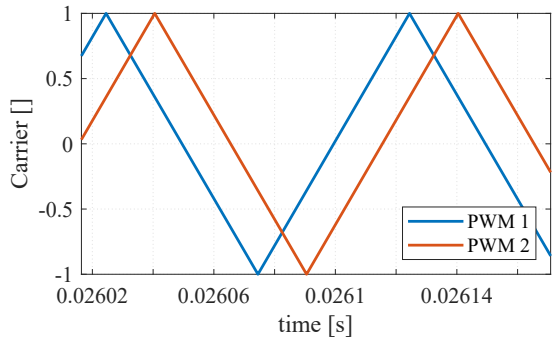


Figure 3.3: PWM carrier offset example

applications either a 3-rd harmonic component is added like discussed in 2. Another way is to add a zero sequence based on the min/max method presented in [80]. This method increases is preferred and used in this study. As a result, the states of the inverter switches are defined as

$$[s_1, s_2, ..., s_{\mathrm{N}}]^{\mathrm{T}} = v_{\mathrm{ref}}(t) > v_{\mathrm{tri}}(t). \tag{3.4}$$

s_{n} denotes the state in which the upper switch in phase leg n and can only assume values of 0 or 1. The lower switch has the inverted state. The phase output currents are defined as

$$i_{\mathrm{out},n}(t) = \hat{I}\sin(\omega t + (n-1)\varepsilon - \phi), n = 1, 2, 3, .., \mathrm{N} \tag{3.5}$$

where ϕ is the phase displacement. Then, the current through the inverter stage as defined in Fig. 3.1 is

$$i_{\mathrm{inv}} = [i_1(t), i_2(t), ..., i_{\mathrm{N}}(t)] \cdot [s_1, s_2, ..., s_{\mathrm{N}}]^T \tag{3.6}$$

where the inverter current composites a sum of the DC link current and capacitor ripple current as defined in Fig. 3.1. This can be expressed as

$$i_{\mathrm{inv}}(t) = I_{\mathrm{DC}} + i_{\mathrm{c}}(t) \tag{3.7}$$

and by further assuming that the capacitor is supplying the AC component of the inverter current and thus the inverter only consumes DC current it is possible to extract the DC current as the average of the inverter current. By rearranging (3.7) it is possible to obtain the capacitor current $i_{\mathrm{c}}(t)$. The RMS value of this capacitor current, I_{c}, is one of the dimensioning factors when deciding the DC link capacitor rating.

The DC link dimensioning of multi–phase inverters can in practice be done in the same way as in the case for the 3 phase inverter discussed above by scaling the phase current as in (3.1).

Capacitor voltage ripple

The other dimensioning factor is the DC link voltage ripple. The C-rating of the capacitor can be estimated by coulomb counting and by imposing a maximum allowable voltage ripple. The stored charge in a capacitor is

$$Q = CV \tag{3.8}$$

where Q is the charge. The equation above can be reformulated as

$$Q(t) = CV_{\mathrm{c}}(t) = \int_0^t i_{\mathrm{c}} dt. \tag{3.9}$$

The voltage ripple is defined as a percentage of the DC link voltage

$$5\% = \frac{\Delta v_{\mathrm{c}}}{V_{\mathrm{DC}}} = \frac{\Delta Q_{\mathrm{c}}}{CV_{\mathrm{DC}}}. \tag{3.10}$$

Therefore by re-arranging (3.10) and by integrating the current as in (3.9) it is possible to obtain the minimum capacitance that will satisfy the voltage ripple in that operating point [69].

Fault operation

The 6-phase configurations are redundant and thus it is possible to operate a vehicle in for example limp home mode if either one of the converters breaks or if there is a fault in one of the star systems of the machine. Hence, the fault condition operation is assumed to be similar to *Case 1* but limited to only half of the original system rating.

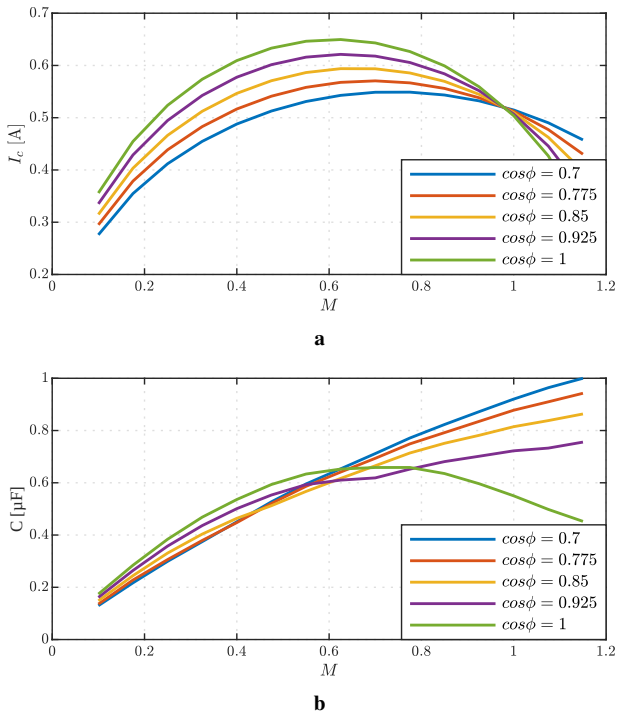


Figure 3.4: Results for *Case 1* considering total inverter operation map

3.3 Case study and results

To yield accurate results the sampling frequency is set 1024 times the switching frequency. No dead-time is considered and ideal switches are assumed. The switching ripples in the output currents are not considered. The 3-phase case is considered as reference and the output currents are set to $1.0\,\mathrm{pu}$. The calculations are implemented in Matlab. The switching frequency only impacts the capacitance rating of the inverter and the rms current rating is independent of switching frequency.

Modelling results Case 1

The maximum simulated rms current stress, I_c, for the 3-phase configuration is shown in Fig. 3.4 and is $0.65\,\mathrm{pu}$ of the phase current, in agreement with theoretical results

from [24], [64].

The minimum capacitance rating that is needed to satisfy the $5\,\%$ voltage ripple is dependent on both the power factor, $\cos\phi$, and the modulation index amplitude, m_{a} and phase current, I_{ph}. This minimum capacitance that satisfies all operation points for the 3-phase inverter bank is set as $1\,\mathrm{pu}$ for further comparisons.

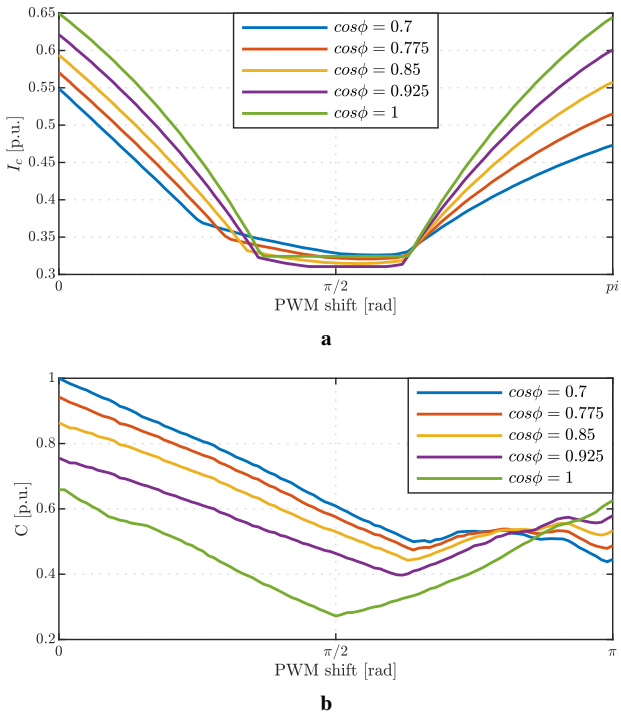


Figure 3.5: Results for *Case 2* considering $\cos\phi = [0.7, 0.775, 0.85, 0.925, 1.0]$

Modelling results Case 2

From results in *Case 1* it can be seen that both capacitor current rating and capacitance rating depend on both the power factor and modulation index. The different surface plots in Fig. 3.5 are for various values of $\cos\phi$ ranging from 0 to 1. Additionally, different values of PWM carrier shift are swept. The carrier wave sweep displays

symmetry after $50\,\%$ (or $180\,°$) displacement, therefore for clarity the plots are limited to only this value of PWM shift.

The global maximum of I_c for each PWM shift is extracted to find the global optimal value of the PWM shift as shown in Fig. 3.5a. The optimum PWM shift value for *Case 2* can be observed at approximately $29\,\%$ amounting to $0.35\,\mathrm{pu}$ capacitor current. If this value is chosen the DC link current stress is reduced by $46\,\%$ compared to the reference *Case 1*.

In the capacitance surface plot in Fig. 3.5b it can be observed that with increased PWM shift the general trend is that the capacitance value to satisfy the $5\,\%$ voltage ripple decreases. In Fig. 3.7b the maximum value of capacitance that satisfies all operation points are plotted as a function of PWM shift. With $0\,\%$ PWM shift the minimum required capacitance is the same as in *Case 1*. It can further be seen that the optimum capacitance value is different from the optimum value for the capacitor current.

Modelling results Case 3

Similaly to *Case 2* the global map of the capacitor current I_c and minimum capacitance for $5\,\%$ voltage ripple is shown in Fig. 3.8. Unlike *Case 2* which only has a global symmetry around $50\,\%$ of PWM shift, *Case 3* exhibits also a local symmetry around $25\,\%$ of PWM shift.

Global maximum of I_c for each PWM shift and power factor are extracted and presented in Fig. 3.6a. Due to the earlier mentioned symmetry around $25\,\%$ of PWM shift minimum value of $0.40\,\mathrm{pu}$ at approximately $15\,\%$ or $35\,\%$. This is a reduction by $38\,\%$ compared to the reference *Case 1* but is larger than *Case 2*.

Unlike *Case 2* there is no monotonous trend in *Case 3* as is shown in Fig. 3.6b. Furthermore, the worst case of PWM shift for *Case 3* is slightly lower than that of *Case 2*. This can be attributed to the phase shift between the star systems.

In Fig. 3.6b it can further be seen that the capacitance rating relatively flat as a function of PWM offset and amounts to approximately $0.58\,\mathrm{pu}$ of *Case 1*.

Fault operation results

Fault operation is only considered for *Case 2* and *Case 3* where in a fault scenario in one of the star systems that system is considered to be disconnected. Since the neutral points are isolated from each other they do not interfere with each other electrically. Therefore, in both *Case 2* and *Case 3* the remaining star system can be mod-

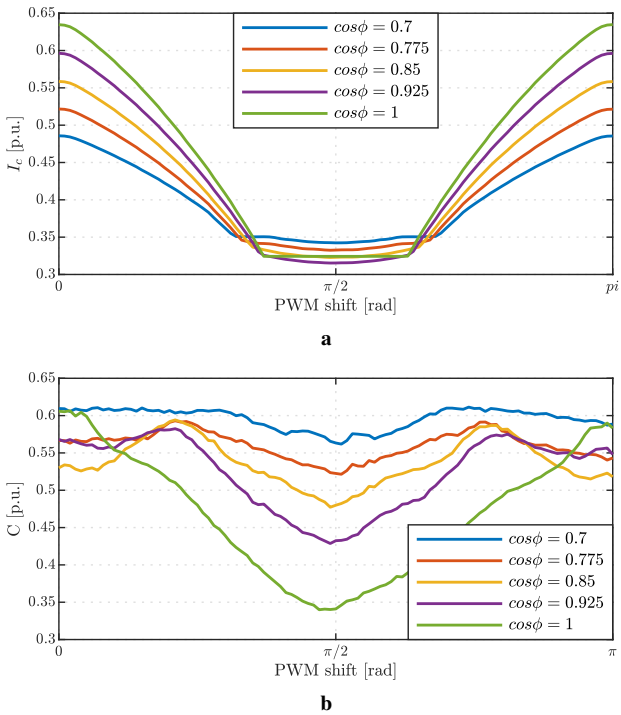


Figure 3.6: Results for *Case 3* considering $\cos\phi = [0.7, 0.775, 0.85, 0.925, 1.0]$

elled as *Case 1* with half the current rating and PWM shift no longer applies. The maximum capacitor current amounts to 0.325 pu and minimum capacitance rating to 0.5 pu which are both less than the optimized ratings of healthy *Case 2* and *Case 3* configurations. A summary of the results is shown in Table 3.1.

3.4 Conclusions

In this chapter the impact of carrier interleaving on the DC link sizing based on the topology of the 12 slot 10 pole FSCW is investigated. The results offer simple guidelines based on the three phase reference case for both current and voltage ripple modelling.

The three phase reference case shows the largest amount of DC link capacitor volt-

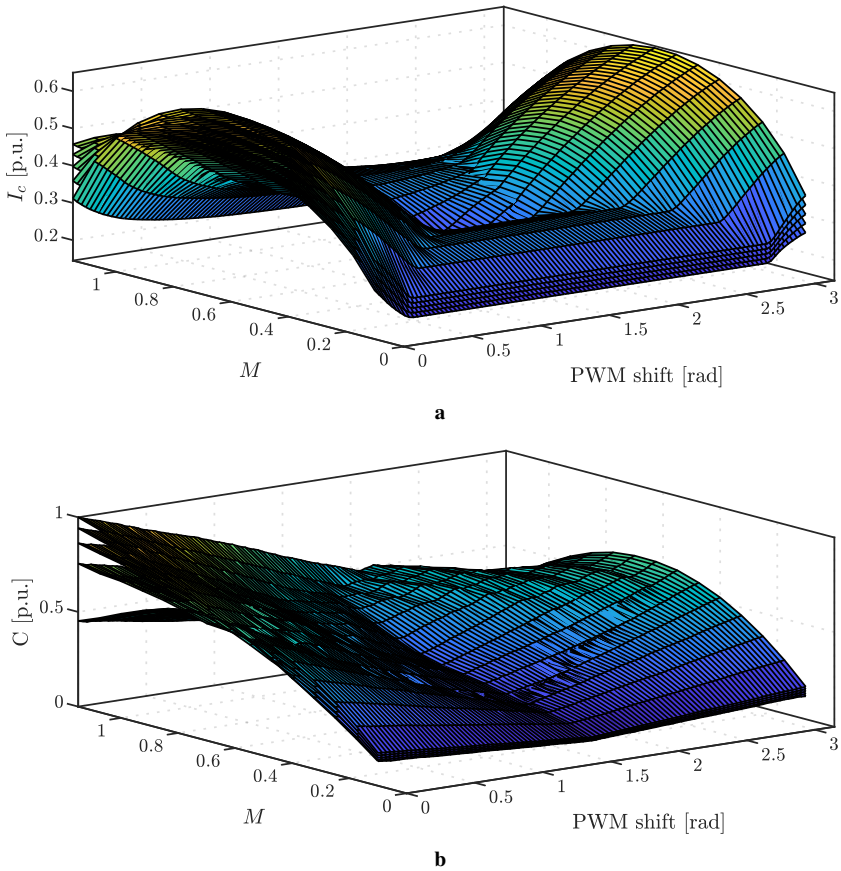


Figure 3.7: Global maps based on the PWM shift for *Case 2*

age and current ripple. The two different 6-phase configurations offer improvement on both current and voltage ripple. Based on the phase shift between the star systems the results for the 6-phase cases vary. The current ripple in *Case 2* with parallel stars has the lowest value. In *Case 2* the voltage ripple is strongly dependent on the value of the PWM shift, on the other hand the voltage ripple in *Case 3* is relatively independent of PWM shift. Despite the sligtly better current stress performance of *Case 2*, *Case 3* might be more traditional and advantageous to use due to better utilization

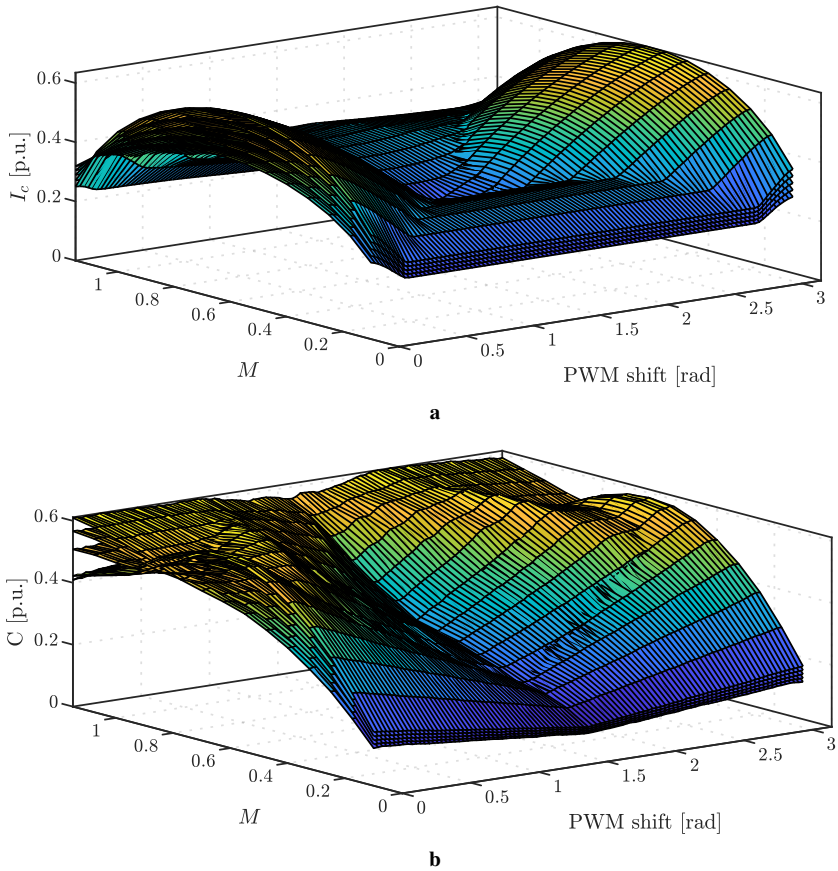


Figure 3.8: Results for *Case 3* considering $\cos\phi = [0, 0.25, 0.50, 0.75, 1.0]$

of the DC link voltage.

In fault operation the worst case capacitor stress is always lower than the optimized values of *Case 2* and *Case 3*. Therefore no over-dimensioning of the DC link is necessary to keep fault safe operation.

Table 3.1: Summary of the results

	Current optimization		Capacitance at opt. PWM
	$I_{c,max}$ [pu]	opt. PWM shift [%]	C_{max} [pu]
Case 1	0.65	NA	1.0
Case 2	0.35	29	0.56
Case 3	0.40	15&35	0.55
Fault	0.325	NA	0.5

CHAPTER 4

High Power Density Inverter for Electric Vehicles Utilizing Surface Mount Components

This chapter presents the electrical and thermal design aspects of a direct cooled Al-PCB for electric vehicle application. At first, the overall performance requirements are discussed, which sets the groundwork for the sizing of the inverter. The sizing is a multiphysics problem with electro-thermal considerations. Next, the design of the half-bridge switching cell is described. Subsequently, the impact of Al-PCB on DC-link design is discussed. Furthermore, the the gate driver interface to the switching cell and current sensing are presented. Lastly, thermal aspects are investigated.

4.1 Design requirement and topology selection

Integrating an inverter with an electric machine has been proposed in the literature [61] - [65]. The different integration concepts can be classified into four categories:

1. Radial Waterjacket Mounted (RWM) [81]
2. Radial Stator Back Mounted (RSBM) [82], [83]
3. End Waterjacket Mounted (EWM) [84]

4. End Stator Mounted (ESM) [85]

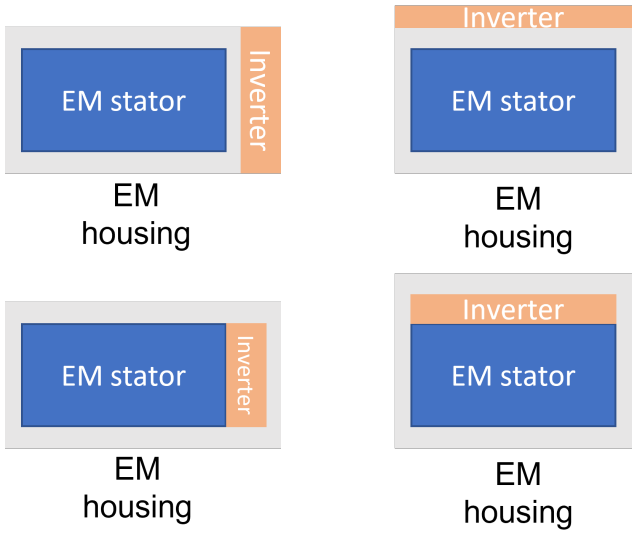


Figure 4.1: The four main types of integration of inverter to the electric machine. Top left EWM, top right RWM, bottom left RSBM, bottom right ESM

RWM means that the inverter part is mounted on to the waterjacket (housing) of the electric machine - shortening cooling ducts and electrical interconnections. RSBM integration is similar in principle but the inverter is integrated even more intimately to the machine on the stator back inside of the machine housing. This is typically associated with larger environmental challenges for the inverter and machine, but could in theory achieve higher power density. Common for radial mount is that it often is advantageous in higher speed applications as these types of motors tend to be longer to reduce rotor inertia. Furthermore, this integration method does not interfere with gearbox integration, and it may be possible to design a shared cooling channel between the inverter and the machine.

EWM are inverters that are integrated onto the end plate of the motor housing elongating the total drive unit. Similarly, ESM integrated drives is similar to EWM but is hosted inside the housing, making it a more high degree of integration a but more environmentally challenging to accomplish. Stator end integrated drives are preferable in high torque applications where the diameter of the machine tends to be larger pro-

viding enough surface space to integrate an inverter. More integrated designs such as stator iron integrated inverters face challenges of confined space and bigger thermal risks than the ones mounted on the machine housing. In some examples integration is co-location of the inverter and machine which means that the inverter's cooling channels and connectors are not integrated [82]. However, integrating cooling structures and connectors could bring additional weight and space savings.

Another essential aspect in safety-critical applications such as EVs is safety and fault tolerance. Two approaches, modularization of the entire integrated drive and altering the electrical configuration of the electric machine to improve fault tolerant operation, are presented in [86]. [87] lists several topologies that improve reliability, such as single-phase inverters or open-ended winding configurations for three-phase motors. Additionally, multi-level inverters can have some fault tolerance, as reported in [88]. Nevertheless, another way to increase redundancy is to increase the number of phases. For example, fault-tolerant drives using five and seven-phase are discussed in [89], [90]. Multi-three-phase drives feature the simplicity and familiarity of three-phase drives and have been proposed in the literature [26], [68], [91].

WBG devices feature several attractive features for inverters in integrated drives. These include low switching losses, low conduction losses, high temperature tolerance and as a result high power density [30]. SiC and GaN devices are both alternatives at face value, however SiC has significantly higher industry maturity at the power level interesting for the automotive industry. Additional benefits of using MOSFET based inverters compared to IGBT based ones especially related to partial load applications has already been discussed in Chapter 2. And the results from such a study is also discussed in Paper III, where it is shown that using a MOSFET based drive-train in multi-phase applications is more advantageous due to lack of forward voltage drop losses. Therefore, the inverter is designed with SiC based MOSFETs.

An interesting technology to explore the feasibility to use discrete components in high power, high power density application is the use of metal core PCBs. Typically such PCBs are used in low voltage LED applications. The base structure is described in Fig. 4.4b. Previous research where this type of PCB technology for motor drive application is limited to either low voltage and lower current applications [20], [22]. These types of PCBs could make a viable alternative to use SMD components. Power modules which are today utilized are thermally optimized but bulky, which could make integrated solutions challenging. In Fig. 4.2 a scatter plot of power modules and discretes vs price is shown. Due to higher production volumes and standardized packaging the SMDs have a median price per $1.36\,\mathrm{kW/EUR}$ compared to $0.67\,\mathrm{kW/EUR}$

for power modules.

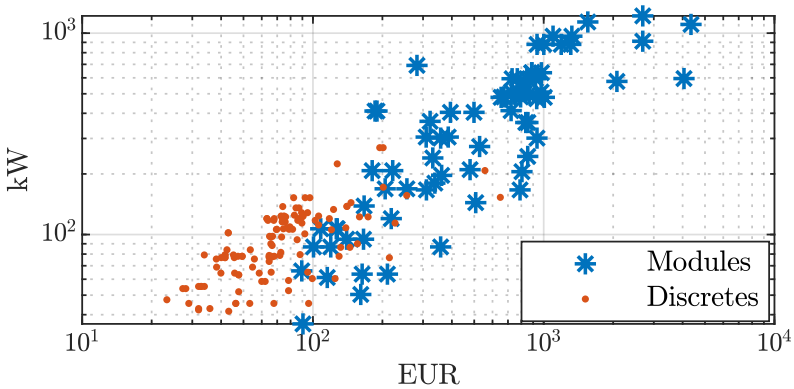


Figure 4.2: Pricing per kW of discrete SiC components vs SiC power modules in the voltage classes spanning 600 V to 1700 V. Prices collected in the spring of 2023

The critical design requirements of the inverter are summarized in Table 4.1. The requirement in this project is to design an integrated inverter solution for a high-power application, e.g., heavy-duty trucks with a maximum power output of $250\,\mathrm{kW}$. The propulsion motor is a permanent magnet synchronous machine (PMSM) with an end plate diameter of $240\,\mathrm{mm}$. The Inverter DC-link voltage is increased to 800V to reduce the required current level, reducing the required copper area and weight. The maximum coolant temperature is $65\,^{\circ}\mathrm{C}$ according to standard automotive benchmarks. The DC voltage ripple limitation is similarly in line with common automotive requirements [92].

4.2 Design of the inverter

This section deals with the detailed design steps of the Al-PCB based integrated drive topology. Including trade-offs and limitations of the technology. At first the geometric constraints are discussed and their impact on the phase leg switching cells. A switching cell in this thesis denotes phase leg including the phase output and the DC link capacitor. Further, the implications of the selected topology and geometry on the capacitor bank design is discussed.

The thermal and heatsink design and modelling is then introduced and the con-

Table 4.1: Inverter requirement parameters

Parameter	Value	Unit
End plate diameter, D	240	mm
Output power, P_{out}	250	kW
DC link voltage, V_{dc}	800	V
DC link voltage ripple, ΔV_{dc}	10	%
Coolant temperature, T_{coolant}	65	°C

straints of the thermal design of the inverter.

Lastly, the experimental verification of the concept is presented.

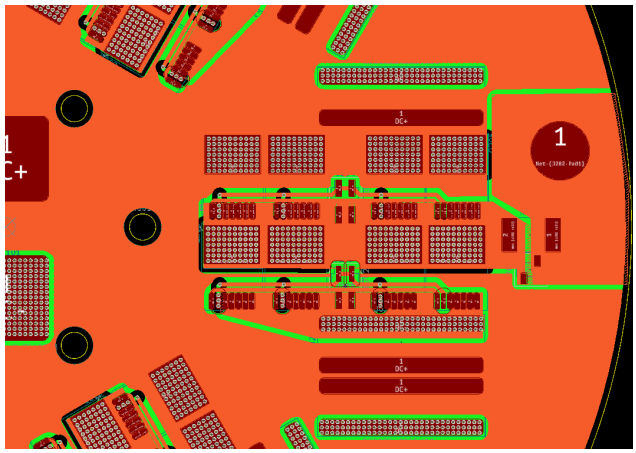
Inverter layout and chip selection

A traditional inverter design with a rectangular layout could be used for end plate integration, as presented in [93]. However, this work selects a circular layout to achieve better space utilization. One challenge in using Al-PCB for a high current application, as reported in [20], is the voltage drop in across the PCB due to a non-symmetric DC link supply. An unbalanced voltage at the different phase legs leads to problems with control and circulating currents. Therefore, the DC link is placed around the circular Al-PCB's geometric center.

The inverter is constructed using six half bridges arranged in a circular layout, as shown in Fig. 4.3. Each half-bridge consists of four parallel SMD SiC chips with D2PAK casing. The switches hav a nominal rating of 1200 V/98 A. The maximum current rating of each chip is rated at a case temperature of 25 °C, which implies a maximum total phase current of 392 A. The chips feature a low turn-on and turn-off loss of 461 µJ and 400 µJ, respectively. Additionally, with an on-resistance of 20 mΩ, the conduction losses can be expected to be lower [94]. The final design is depicted in Fig. 4.10.

Design of the half bridge switching cell

An important aspect in design of a half-bridge with multiple chips in parallel is uniform distribution of current. If the current sharing is not equal, the losses can be



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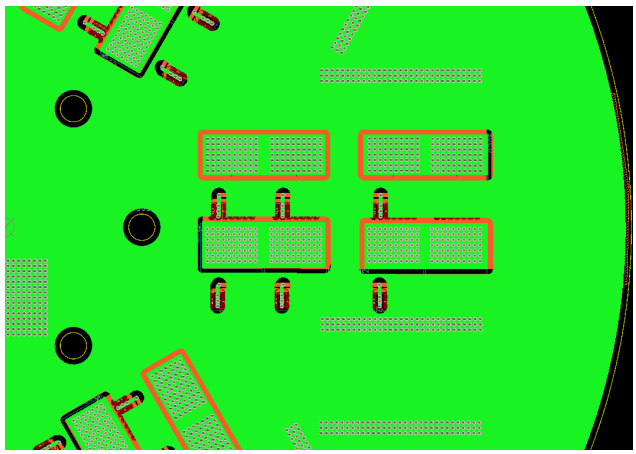


b

Figure 4.3: PCB layer design. The gate driver pin is placed in the middle for symmetry reasons. (a) top copper layer, (b) bottom copper layer with thermal vias.

un-even and certain switches might operate above their recommended specification. Since the half bridges are constructed along a circular shape and the DC terminals are selected to be in the middle, and there is a fictitious center point from which the current can be considered originating. It is best practice to design the layout for current sharing purposes so that the current from source to sink, in this case, the middle point

Table 4.2: Aluminium PCB design parameters

Parameter	Value	Unit
Top copper thickness, $T_{\mathrm{Cu},1}$	140	µm
Top dielectric thickness, $T_{\mathrm{Diel},1}$	100	µm
Bottom copper thickness, $T_{\mathrm{Cu},2}$	35	µm
Bottom dielectric thickness, $T_{\mathrm{Diel},2}$	100	µm
Aluminium thickness, T_{Al}	1.6	mm
Dielectric thermal conductivity, σ_{thl}	3.8	W/mK

and phase output, is equidistant for both the top and bottom side switches. To ensure that the loading of the capacitors stays as even as possible similar design approach is taken for the capacitor bank. In Fig. 4.4a two examples are shown, one where the distance between input and output terminals is equidistant and an even current sharing is achieved. On the other hand, if the distance between the terminals is not equidistant through the switches, some switches may end up carrying more load than their neighbouring switches.

To improve cell inductance the choice here is to implement a two layer structure with the top layer copper layer being of positive polarity and the negative polarity being the bottom copper layer. This way flux cancellation can be achieved minimizing the inductance of the inverter and the switching cell, as indicated in Fig. 4.4b where the towards and return paths are on top of each other and carry current in different directions. The choice of a two layer PCB comes with the penalty of thermal characteristics. The selected high thermal conductivity dielectric is VT-4B from Ventec with thermal conductivity of $3.8\,\mathrm{W/mK}$. To reach the necessary electrical insulation levels between the layers $100\,\mu\mathrm{m}$ is selected which according to the datasheet should withstand $4000\,\mathrm{V}$ [95]. The final PCB design is summarized in Table 4.2.

Capacitor sizing selection

Metallized film capacitors are most commonly used for drives. These capacitors offer a moderately high current rating at a relatively high capacitance rating. Typically modern inverters employ switching frequencies of more than $10\,\mathrm{kHz}$ and therefore when sizing a capacitor bank in fact the limiting factor is the current rating of the ca-

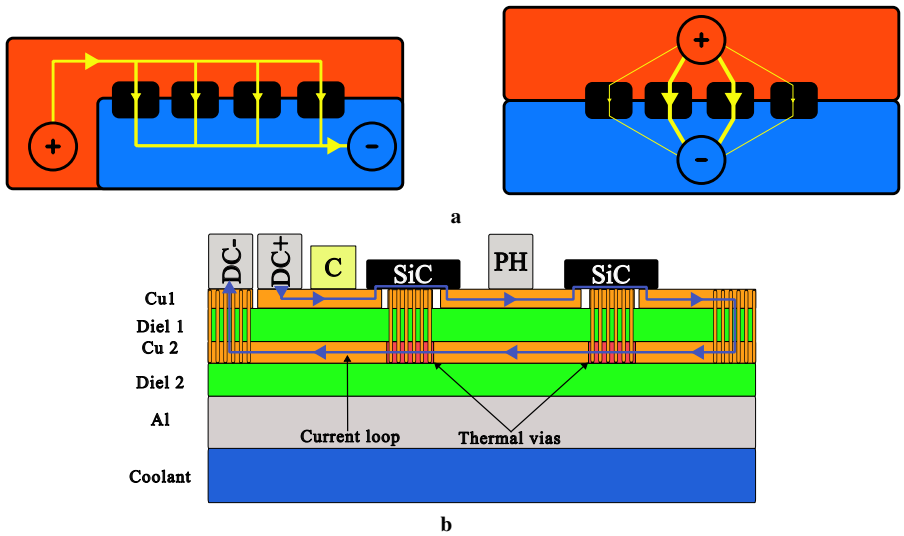


Figure 4.4: Switching cell design considerations. (a) top view - it is important to ensure that the current path is equidistant when parallelling switches, (b) layer view - illustration of how flux cancelling is achieved

pacitor bank. Film capacitors are temperature sensitive devices and they are mounted on copper bus bars either by soldering or mechanical fixings [30].

Ceramic capacitors offer high temperature stability and high current ratings but low capacitance. High temperature capability of these capacitors makes them applicable for automatic SMD assembly. For this reason the capacitors from the CeraLink series by TDK are explored. A series of numerical simulations for a DTP configuration at maximum output current defined by data in Table 4.1 across multiple switching frequencies is performed. A set of plots similar to Fig. 3.8 is produced and the worst case for $C_{\min}$ that still satisfies the ripple goals defined by the system is extracted. The results can be seen in Fig. 4.5. Only the capacitance rating required to meet the system requirements changes with frequency. Due to space constraints it is decided to use three $2.5\,\mu\text{F}$ CeraLink capacitors per switching cell. Total effective capacitance at $800\,\text{V}$ rating is therefore $23.4\,\mu\text{F}$. Hence, at least $40\,\text{kHz}$ is required to operate the inverter within system specifications.

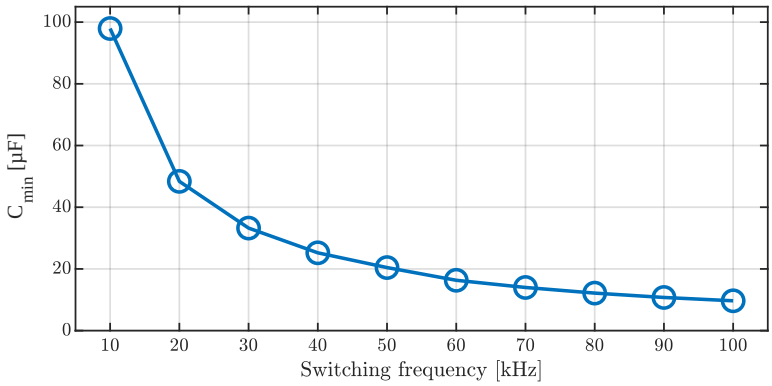


Figure 4.5: Minimum required capacitance vs switching frequency to satisfy the requirements in Table 4.1

Heatsink design

In the automotive industry glycol-water cooling is standard in inverters and electric motors. The direct cooling method is preferred as it avoids the Thermal Interface Material (TIM) which typically contributes to a large thermal gradient, although exceptions exist [21], [32]. When using the Al-PCB it is possible to avoid the TIM and make a direct water-cooled application as the aluminium layer is electrically not active. Direct cooled power modules often have extrusion material, so called pin-fins or ribbon-fins as studied in Paper I, to improve cooling performance. In the case of Al-PCB there is no possibility to create such strcutures in the manufacturing process. It would be possible to improve the cooling by applying ShowerPower concept as developed by Danfoss [96], it was however deemed to be outside of the scope of this concept study.

A cooling channel for the liquid is designed as an engraving into the motor housing. The width of the trench is mandated by the width of one switching cell. To determine the amount of parallel switches at first the estimation of the thermal resistance is done by estimating parameters in a thermal 1-D as shown in Fig. 4.6. The thermal parameters are then used together with the maximum temperature of the switch [94]. At first the maximum temperature gradient from the junction to the heatsink is calculated as

$$\Delta T = T_{\mathrm{j}} - T_{\mathrm{c}} \tag{4.1}$$

where T_j and T_c are the maximum junction and coolant temperatures respectively. Then the total thermal resistance is supposed as a sum of each layer in the thermal stack and is estimated as

$$R_\mathrm{tot} = \Sigma_i \frac{d_i}{\sigma_i A} \tag{4.2}$$

where d_i is the thickness of each layer, σ_i is the thermal conductivity and A is the effective area of the heat dissipation per switch. Once these parameters are calculated the maximum allowable power loss per switch is calculated as

$$P_\mathrm{loss} = \frac{\Delta T}{R_\mathrm{tot}}. \tag{4.3}$$

The results of this analysis are shown in Fig. 4.7. It can be seen that apart from the coolant temperature, the largest temperature gradient limiting the maximum allowable loss is the dielectric materials. After that, the D2PAK switch itself is the second largest temperature gradient followed by the solder layer. It is therefore really important to control the solder layer and the dielectric materials to improve the thermal dissipation of this system. Therefore, to improve the heat dissipation of the dielectric, thermal vias are created in the top dielectric top layer shown in Fig. 4.4b. The thermal vias allows to short circuit the thermal gradient across the top dielectric layer.

The equivalent total thermal resistance is used with the analytic loss calculation method presented in section 2 is used to evaluate the thermal performance of the heatsink. The DC link capacitance value is selected to be $23.5\,\mu\mathrm{F}$ as per the design presented earlier. The total loss per switch and junction temperature of the switch for different power factors and switching frequency are shown in Fig. 4.8. From the figure, it can be seen that even with the switching frequency of $100\,\mathrm{kHz}$, the junction temperature of the switch is below $175\,^\circ\mathrm{C}$.

The resulting design discussed above is shown in the CAD in Fig. 4.9. To verify the above 1D calculations a 3D model is built to be verified numerically using the FEM tool Comsol Multiphysics. The injected power loss per switch is here set to

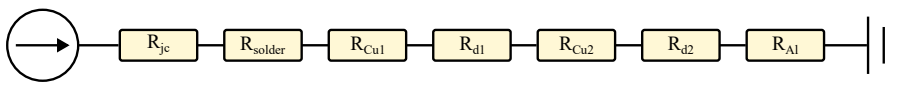


Figure 4.6: Model of the thermal resistance network for an Al-PCB

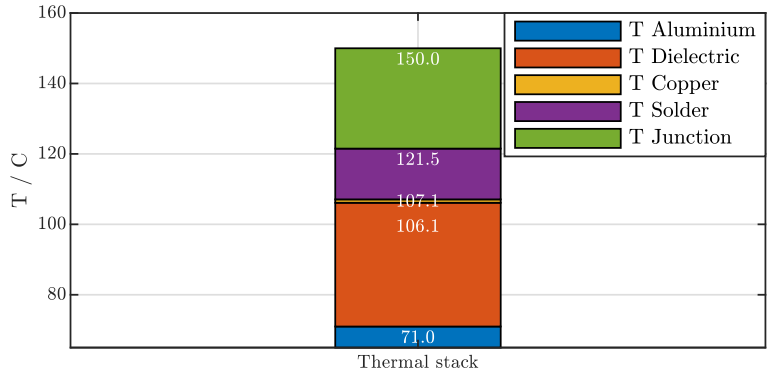
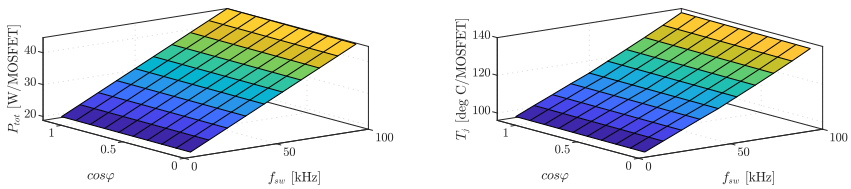


Figure 4.7: Result of 1-D thermal stack



a **b**

Figure 4.8: Results of the analytic modelling. **(a)** Loss per switch at maximum output current. **(b)** Associated junction temperature at maximum output current

40 W and the bottom side boundary condition is set to 65 °C. It is clear that simply using the 1D model would significantly underestimate the thermal spreading effects of the switches through the copper layers - improving cooling. The thermal design estimates are summarized in Table 4.5

Gate driver

For SiC switches the gate driver design is very important. Reliable switching operation is necessary for safety. For traction voltages of 400-800 V isolated gate driving is used. The logic side is normally 5 V whereas the driving side operates at 20/−5 V. The negative gate voltage is especially important in fast switching applications such as the SiC MOSFET due to the high values of $\mathrm{d}V/\mathrm{d}t$ which can cause false turn-on

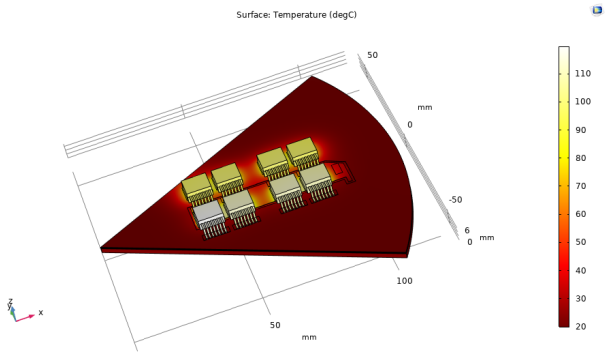


Figure 4.9: Thermal CAD results from Comsol Multiphysics simulation

events. These aspects add the amount components in the gate driver circuit.

Because the SiC MOSFETs dynamic characteristics are so quick it is important that the device parameters are as equal as possible. Some can be hard to control, such as parameter spread between the various switches from manufacturing. In this case it is recommended that the designer uses switches from the same manufacturing batch. Some parameters that can be controlled by the designer are for example gate routing when parallelling switches. Manufacturers advise that the signal is as symmetric as possible [97].

Current measurement

The output terminal of the inverter operates at DC link voltage, hence special consideration when designing current measurement circuitry must be taken in order to transfer the signal to the low voltage side. Typically, Hall effect sensors are popular in EV inverter applications because, by the nature of the measurement, they are electrically isolated [98]. However, such sensors can be bulky when measuring currents in the hundreds of amperes [98]. Other more integrated types of Hall effect sensors are also available such as the ones from Melexis, which incorporate Hall effect sensor measurement with a small footprint on the PCB. However, this technology requires a special output busbar that is routed in a specific manner. To avoid this complexity, the selection in this thesis application uses a shunt current measurement utilizing a low-resistance resistor with high power dissipation and low thermal resistivity coefficient. The choice is to utilize the WSLP3921 $100\,\mu\Omega$ resistor from Vishay with the $\pm 50\,\mathrm{mV}$

Table 4.3: Al-PCB prototype data

Parameter	Value	Note
Topology	2-level, 6-leg	Two layers
Switches	$1.2\,\mathrm{kV}/98\,\mathrm{A} \times 36$	NVBG020N120SC1 [94]
Capacitors	$2.5\,\mu\mathrm{F} \times 18$	B58035U9255M001 [100]
Current sensor	$100\,\mu\Omega$	WSLP3921 [101]
Cu layers thickness	$140\,\mu\mathrm{m}/35\,\mu\mathrm{m}$	Layer 1 / Layer 2
Dielectric thickness	$100\,\mu\mathrm{m}$	Ventec VT-4B [95]
Inverter size (DxH)	$240 \times\ 28\,\mathrm{mm}$	Incl. gate driver, excl. heatsink
Heatsink size (DxH)	$240 \times\ 20\,\mathrm{mm}$	Excluding inverter

AMC3302 reinforced isolated amplifier. This configuration is, therefore, capable of detecting currents up to $500\,\mathrm{A}$ [99].

4.3 Experimental setup

With the above considerations in mind an Al-PCB inverter was constructed. The direct cooled inverter with the accompanying heatsink can be seen in Fig. 4.10. The heatsink is thought to be the endplate of the electric motor housing which has been modified with cooling channels for the inverter. The final inverter bill of materials is summarized in Table 4.3. The total inverter volume amounts to $2.17\,\mathrm{dm}^3$

In order to verify the thermo-electrical design procedure described in the previous sections an experimental setup is constructed. The thermal performance is characterized by injecting a known current from a DC power supply to the top switch position from positive DC rail to phase output while $V_{\mathrm{GS}} = 20\,\mathrm{V}$ and measuring the voltage drop across the switches. The same procedure is then repeated for the negative side switch.

The switch temperatures are recorded using 4-W PT-100 sensors which are placed on the top side of the drain side copper terminal as close as physically possible to the actual switch as shown in Fig 4.11. The coolant temperature is measured using 3-W PT-100 at the inlet and outlet of the inverter and the average of the recorded values is

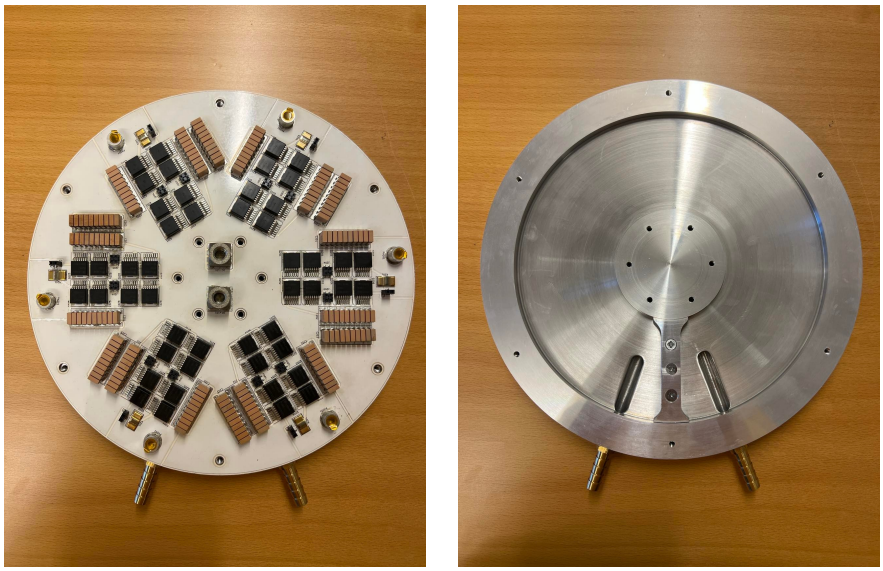


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Figure 4.10: Photo of the Al-PCB inverter and the direct cooled heatsink.

Table 4.4: Temperature measurement instrumentation and setup

Device	Manufacturer	Model	Remark
DC supply	Delta Elektronika	SM 30-200 [102]	-
DAQ	Fluke	2638A Hydra [103]	-
Voltmeter	Fluke	115 [104]	-
Temp. probe	RS Pro	4-wire [105]	Switch temp.
Temp. probe	Unknown	3-wire	Coolant temp.
Flow meter	Swissflow	SF800 [106]	

used. The list of measurement equipment is summarized in Table 4.4.

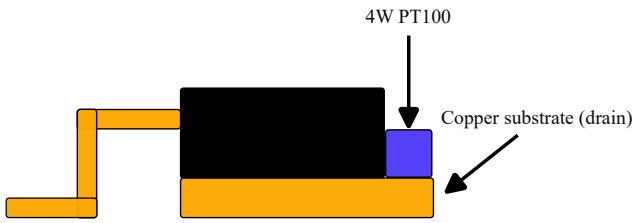


Figure 4.11: Junction temperature estimation point

4.4 Thermal measurements

The thermal measurements were conducted by sweeping the applied currents and recording the coolant temperatures as well as the relevant switch temperatures. The recorded results for top and bottom switches respectively are shown in Fig. 4.12. The y-axis depicts the ΔT gradient as calculated by Eq. (4.1). As the coolant temperature was around $\approx 7\,^{\circ}\mathrm{C}$, relatively large values of ΔT were achieved. Each measurement point was recorded for approximately $120\,\mathrm{s}$ at steady state temperature. At maximum injected current of $190\,\mathrm{A}$ a voltage drop of $1.45\,\mathrm{V}$ was recorded across the 4 parallel swiches, resulting in an average of $69.9\,\mathrm{W}$ dissipated power per switch.

A closer look on how the individual switch temperatures are deviating from the average MOSFET temperature is shown in Fig 4.13. It can be seen that a temperature deviation of $\pm 5\,^{\circ}\mathrm{C}$ is recorded for both top and bottom switch positions. The outliers with the highest temperature deviations from the mean are the middle MOSFET positions for both top and bottom switch position.

The measurement procedure above is repeated for various flow rates. Based on the maximum recorded hot-spot temperature a value for $R_{\mathrm{th,tot}}$ is calculated using Eq. (4.3). $R_{\mathrm{th,tot}}$ denotes the equivalent thermal resistance as if each switch position were one switch - similarly to how it is reported in datasheets for power modules. To obtain *per switch* equivalent one has to multiply these values with 4 and are reported in Table 4.5.

In Fig 4.14 it can be seen that with increasing injected current/power the total value of thermal resistance decreases. This is likely due to improving resolution of the measurement. Another observation is that there is no major difference between bottom and top switch position like predicted in the FEM calculations. This can probably be at least partially attributed to the fact that the thermal vias are modelled as a solid copper pad between the copper layers. In reality the vias are more akin to copper

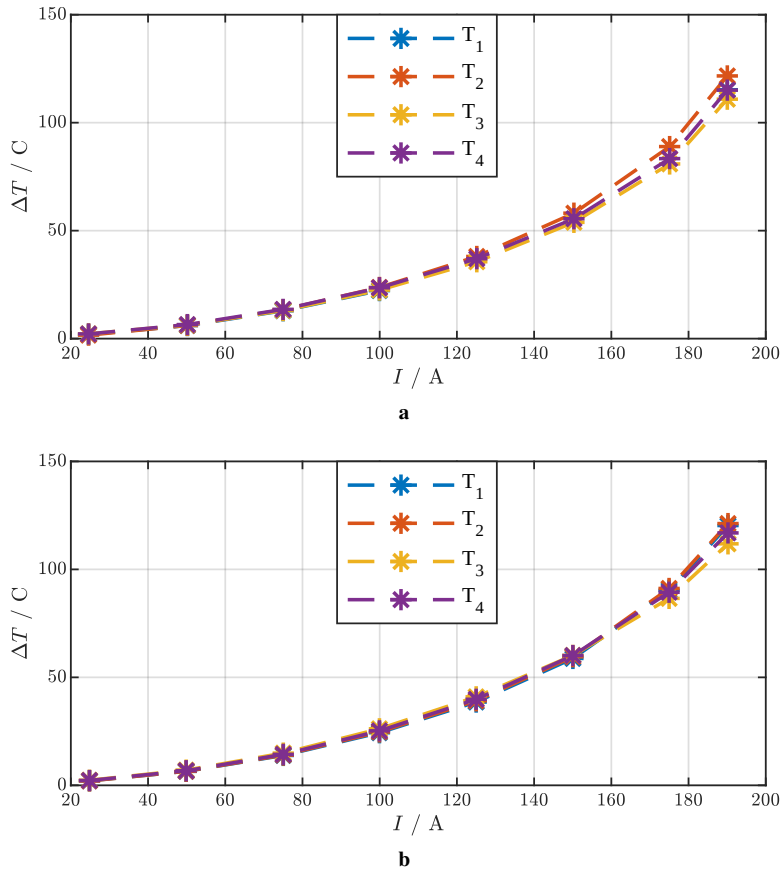


Figure 4.12: Temperatures of the top (a) and bottom (b) switch temperatures at various injected current levels at a constant flow rate of $2\,\mathrm{L/min}$

pipes, which makes their thermal conductivity worse. Nevertheless, if *per switch position* thermal resistance values of $0.37\,\mathrm{K/W}$ are compared to similarly rated direct cooled IGBT or MOSFET modules with pin fin strucutres, a figure of merit is roughly $0.110\,\mathrm{K/W}$ [107].

In order to estimate if the specification is still fulfilled, the measured value of R_{th} is applied in the analytic formulas with temperature feedback from Chapter 2. The coolant temperature and output current requirements from Table 4.1 are used as in-

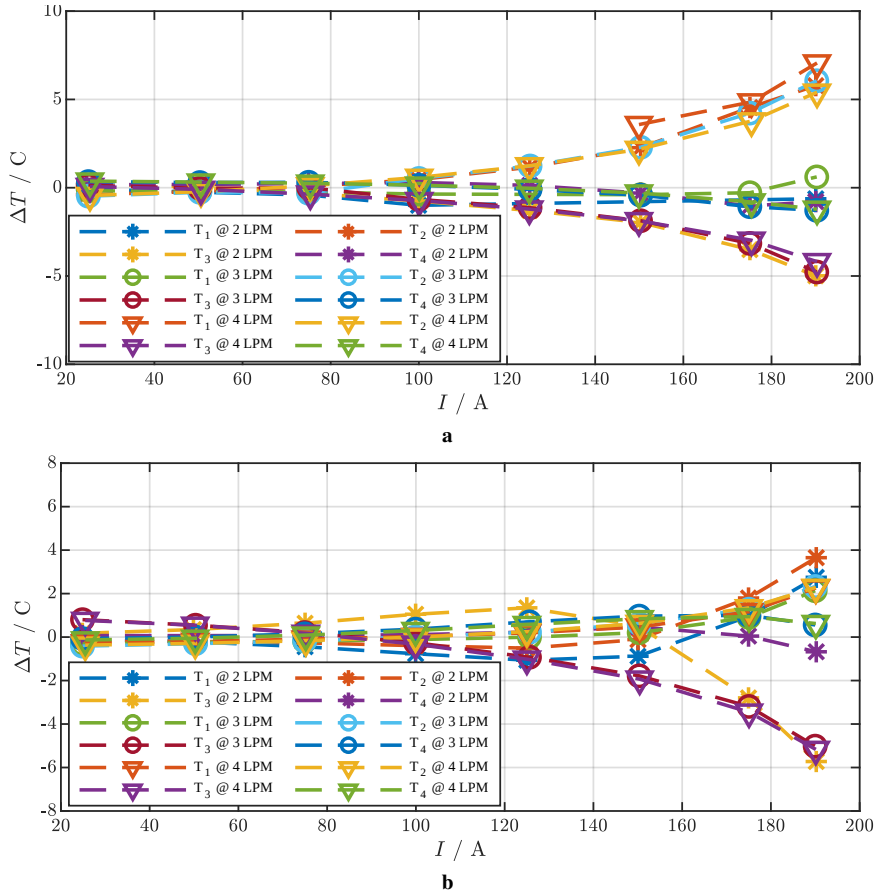


Figure 4.13: Temperature spread of the top switches, (a) and bottom switches (b), when injected with a DC current at $V_{\mathrm{GS}} = 20\mathrm{V}$ at a constant flow rate of $2\,\mathrm{L/min}$

puts. As a result, a safe area of operation within the termal limits of the switches is obtained as shown in Figs. 4.15. It can now be seen that it is no longer possible to switch above $70\,\mathrm{kHz}$ for all operating areas. However, using the previous results of the capacitor dimensioning, switching frequencies above $40\,\mathrm{kHz}$ satisfy the capacitor bank dimensioning.

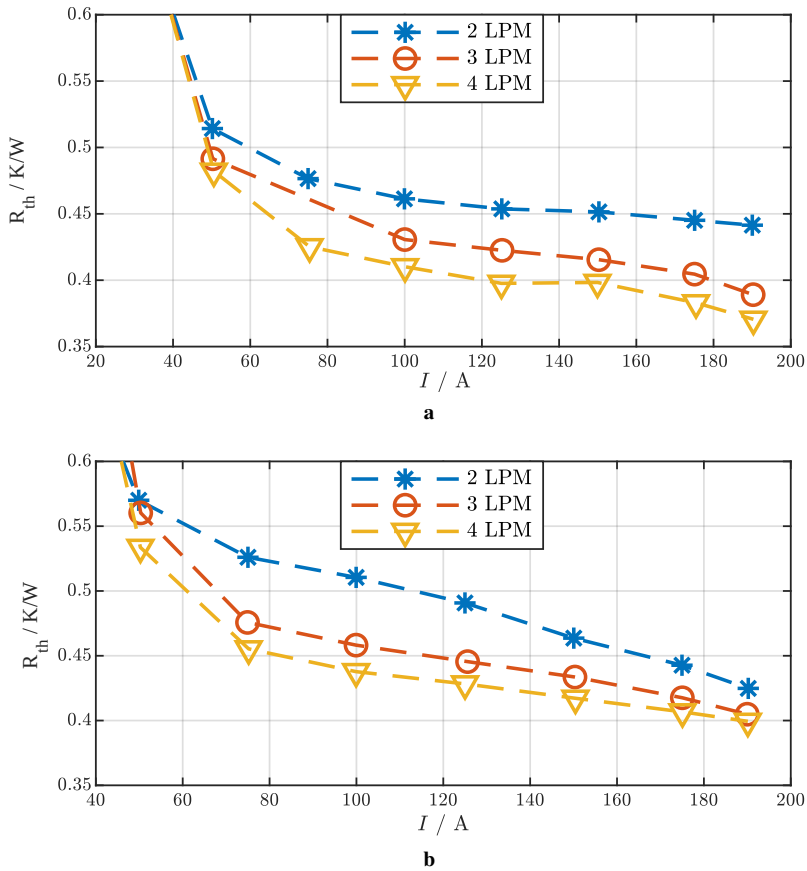


Figure 4.14: R_{th} for various loads and flow rates. (a) top switch. (b) bottom switch

4.5 Switching operation

The electrical measurements are conducted in three phase mode. This is because while conducting the thermal bench-marking, one of the phase legs got damaged. In practice this means that PWM shifting cannot be verified. However, in modelling it is shown that regardless of PWM offset, the DTP assymetric configuration with a $\pi/6$ offset between the three-phase pairs features a halving of the required total capacitance. Hence if a three-phase pair can be operated at nominal capacity it can

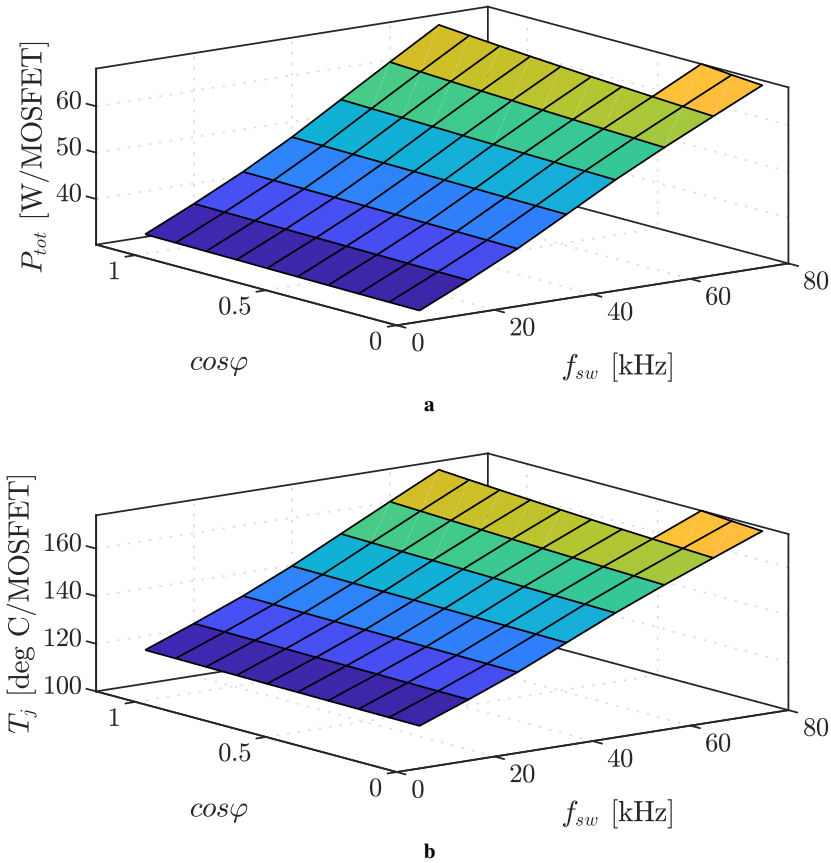


Figure 4.15: Updated modelled losses and junction temperatures ($T_\mathrm{j} < 175^\circ\mathrm{C}$) using measured value of thermal resistance, (a) losses per switch (b), junction temperature

be assumed the DTP can be assumed to be withing specification.

The three-phase operation is conducted using a 300 V-30 A DC supply and a three phase L-load. The PWM and control signals are generated by a dSpace system. The load inductances are measured with an LCR-meter to be approximately $0.8\,\mathrm{mH}$ and the switching frequency is set to $40\,\mathrm{kHz}$. The open loop three phase operation waveforms are depicted in Fig. 4.16 and Fig. 4.17. At -5 and $0\,\mathrm{ms}$ there are mis-trigger events where the gate-driver does not trigger for one switching period. In this instance

the system becomes unbalanced and a zero sequence is observed. In the other time instances the currents and voltages behave as expected with relatively low DC side ripple. The tests are limited by the mistrigger events which increase with increased DC link voltage. Therefore, the maximum output current that could be measured is limited by the applied DC voltage of $50\,\mathrm{V}$.

4.6 Conclusions

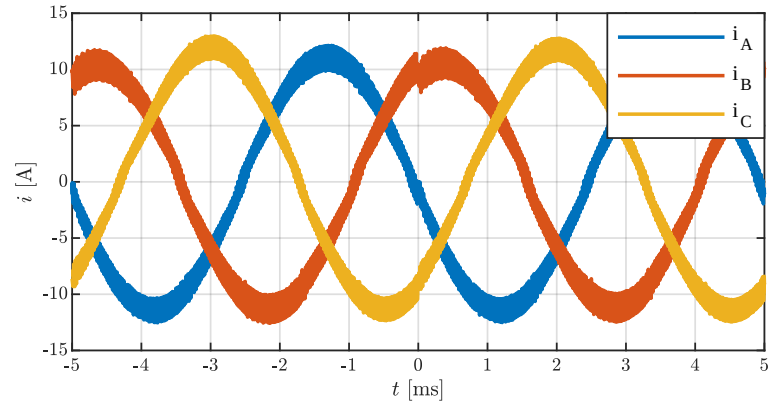
In conclusion, the Al-PCB technology could be beneficial in integrated drives considering the low price per ampere of the D2PAK chips. High geometric flexibility during design process as well high degree of automatizing during manufacturing this technology offers an attractive alternative to power modules.

The thermal dissipation capabilities in a direct cooled Al-PCB could according to measurements and calculations deliver up to $250\,\mathrm{kW}$ output power - resulting in a volumetric power density of $95\,\mathrm{kW/dm^3}$.

One of the drawbacks of this solution is that it relies on low-C ceramic SMD capacitor technology and hence a high switching frequency to operate within voltage ripple specifications. This leads to additional switching losses in the MOSFETs and reduces the efficiency of the inverter.

Table 4.5: Al-PCB thermal resistance per switch modelled and measured

Parameter	Value	Unit
Analytical thermal resistance, $R_{\mathrm{th,an}}$	1.16	K/W/MOSFET
Numerical thermal resistance, $R_{\mathrm{th,num}}$	0.74	K/W/MOSFET
Measured thermal resistance, $R_{\mathrm{th,meas,top}}$	1.48	K/W/MOSFET
Measured thermal resistance, $R_{\mathrm{th,meas,bot}}$	1.60	K/W/MOSFET



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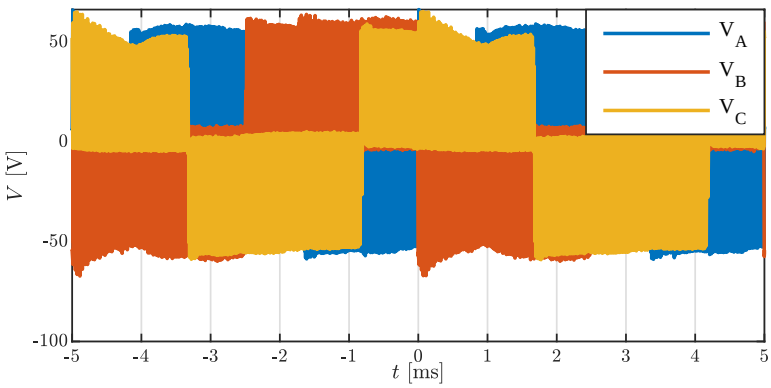

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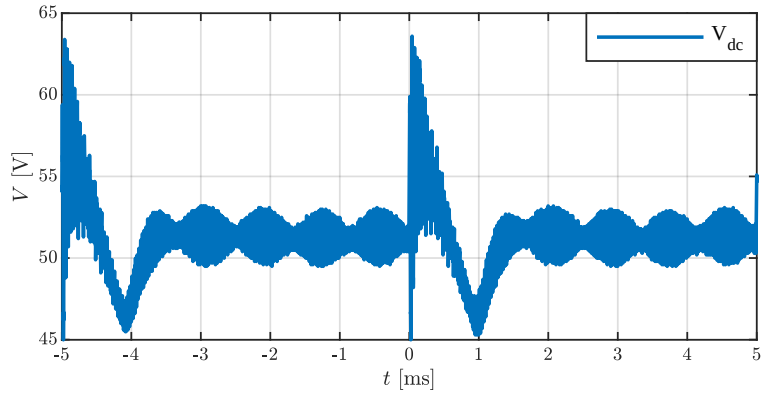
Figure 4.16: Measured waveforms, (a) phase currents (b), phase voltages



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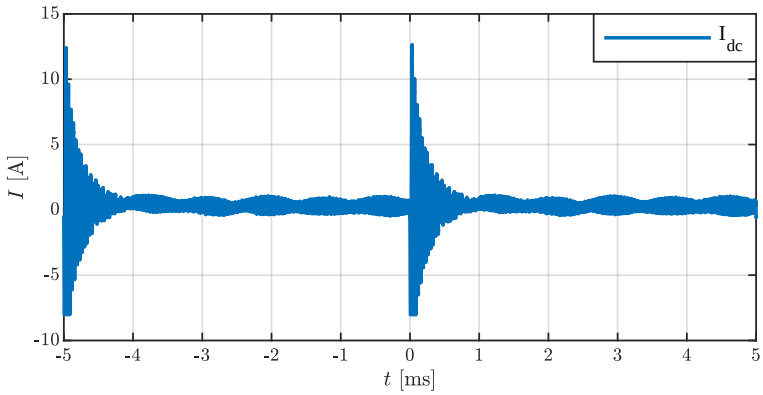

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Figure 4.17: Measured waveforms, (a) DC link voltage (b), DC link current

CHAPTER 5

Conclusions and future work

In this work the modeling, design and practical implementation of a highly power dense inverter is presented. At first a method to analytically calculate losses in MOSFET semiconductors is presented and verified both in simulations and experiments.

5.1 Conclusions

An overview of capacitor modelling is presented, where both the capacitance and current rating requirements are considered. It is concluded that the capacitor bank is an environmentally sensitive component that also has a large relative space-claim in modern drive systems. An implementation of multi-phase drive systems is identified way to reduce the capacitor bank current as well as capacitance requirements by employing carrier wave interleaving. This way the capacitor bank can be downsized by ca. $45\,\%$ in terms of current rating and capacitance rating. These results suggest that if an increase of the switching frequency to $40\,\mathrm{kHz}$ is allowed - compact high temperature, low C-rate ceramic capacitors could be a viable alternative to today's metallized film capacitors.

Based on the modelling results a prototype utilizing discrete components on a direct cooled aluminium based PCB plate is developed. This type of assembly features only

surface mounted components which offer the following advantages:

- high customizable geometries of the inverter are possible
- high level of assembly automation is possible for high volume applications
- high heat dissipation characteristics relative to traditional SMT applications due to elimination of the thermal grease layer.

The results from the thermal tests of this assembly show that a high loss dissipation is achieved for for the designed inverter and that a double three phase inverter topology can be a candidate for high power density integrated motor drives.

5.2 Future work

There are more topics of interest that could be investigated for highly compact drives, such as

- Further research about DC link sizing with respect to distributed DC capacitors and the impact of bus bar parasitics on the performance of the DC link capacitors.
- The mechanical integrity of a metal core PCB mounted directly on an electric machine over a wide range of vibrations experienced in a vehicle and different operating temperatures.
- The possibility to incorporate copper filled thermal vias for better thermal dissipation of the semiconductor losses.
- The EMI and compatibility of an SMD based drive and developing strategies to make this drive qualify for standards in automotive applications.

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