SIS technology development to serve Next Generation receivers for ALMA

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***Abstract*— Modern radio astronomy demands for broadband receiver systems. For SIS mixers, this translates into objective to employ superconducting tunnel junctions with a very low R_nA and low specific capacitance. The traditionally used Nb/AlO_x/Nb junctions have largely approached their physical limit of minimizing those parameters. It is commonly recognized that it is AlN-barrier junctions, which are needed for further progressing of the broadband SIS mixer instrumentation for radio astronomy. In this work, we present the progress in development of the process for high quality Nb/Al-AlN/Nb superconducting tunnel (SIS) junctions' fabrication and their characterization in terms of their specific capacitance.**

Keywords—SIS junctions, AlN tunnel barrier, specific capacitance

I. Introduction

We are developing SIS process technology capable of fabricating mixer chips for Next Generation ALMA receivers. The requirements for such SIS process technology stems from the ALMA 2030 Development Roadmap document [1] calling for twice or triple enhancement of the RF and IF bandwidths of the receivers and consequently the SIS mixers. This in turn translates into the requirement for SIS junctions to have a smaller specific capacitance, C_s, (i.e. junctions with AlN tunnel barrier) and having smaller size.

We have earlier reported on the process development for high-quality Nb/Al-AlN/Nb junction fabrication based on microwave plasma nitridation [2]. We showed that the Nb/Al-AlN/Nb junctions with R_nA product down to ~5 Ohm·μm^2 demonstrate excellent quality. Also, we showed that the produced junctions were quite stable against the thermal annealing, at least up to 200°C, thus allowing for thermal impact during almost any possible fabricating or packaging technology processes.

In this manuscript, we present results of the Nb/Al-AlN/Nb junction process development aiming for fabricating of smaller area junctions, as well as the specific capacitance measurements following the approach similar to that reported in the papers [3] at GARD and in [4] in NAOJ, by means of on-wafer capacitance measurements with 4K probe station.

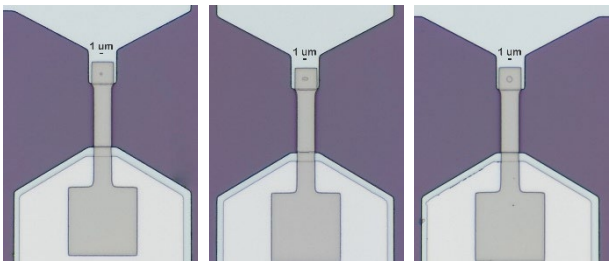

Fig. 1. Micrographs of the Nb/Al-AlN/Nb SIS junctions of different sizes and shapes.

II. Results

We have developed the process capable of fabricating the Nb-based SIS junctions with the junction size achieving junction dimensions ≤1μm^2. We have employed direct laser writing for definition of the junction pattern. After setting up the direct laser exposure process with the AR-N 4340 negative tone resist, the rest of the small SIS junction process has been integrated and the test junctions have been fabricated. The test wafer included the junctions of different shapes and sizes (Fig. 1), as well as the bigger sized round junctions for extracting of the R_nA product along with the junction size offset due to the lithography and etching processes (Fig. 2). The presented on the Fig. 3, the current voltage characteristics of the fabricated submicron Nb/Al-AlN/Nb junctions demonstrate their excellent quality.

Earlier, we reported on the Nb/Al-AlN/Nb junctions specific capacitance measurements [2]. The latter was performed in the test cryostat with long and inevitably lossy stainless-steel coaxial cables connecting device under test at 4K physical temperature with VNA. Use of the cables is largely affects the accuracy of the measurements because the losses and electrical length of the cables are changing while cooling and make the VNA calibration compromised.

Direct measurement of the junction capacitance in cryogenic probe station at NAOJ [4], [6] is seen as a very attractive alternative option both from the point of view of a quicker throughput and - importantly - higher accuracy.

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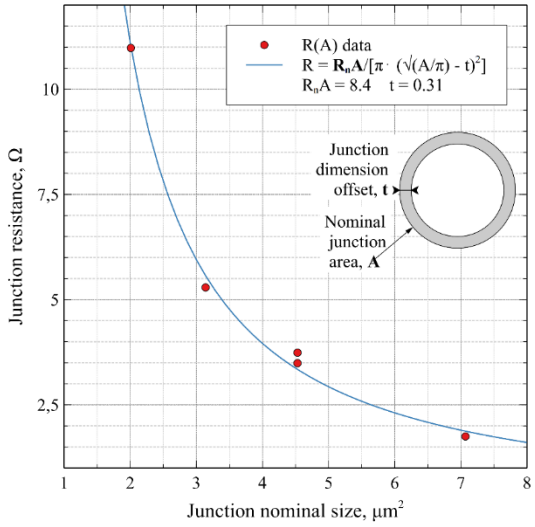

Fig. 2. True R_nA and dimension offset t is extracted from the scaling of junctions' Rn vs nominal area of the test round junctions.

Shown on the Fig. 4, a cryogenic probe station at NAOJ allows to calibrate out all embedding circuitry down to the junction itself. Moreover, through careful design of the test structures on-wafer, we have all three

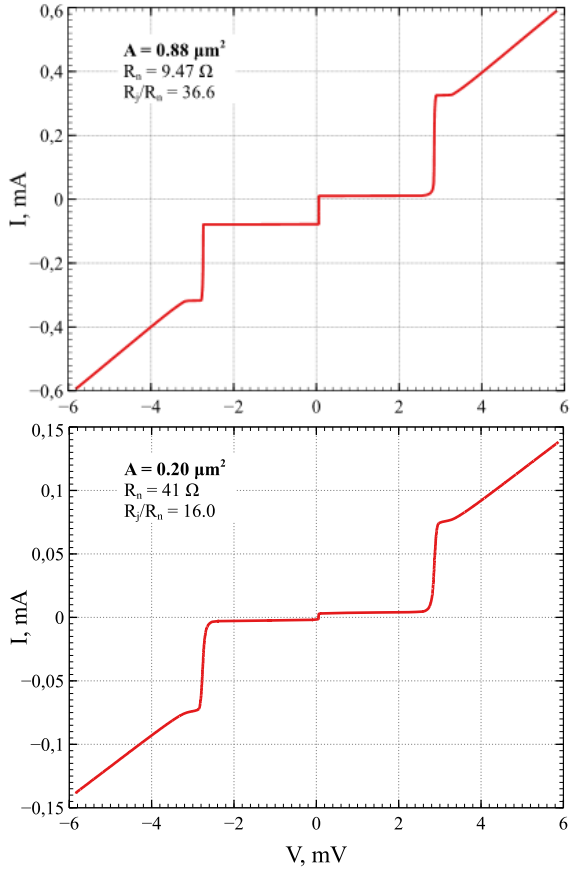

Fig. 3. Typical current-voltage characteristics of the Nb/Al-AlN/Nb junctions.

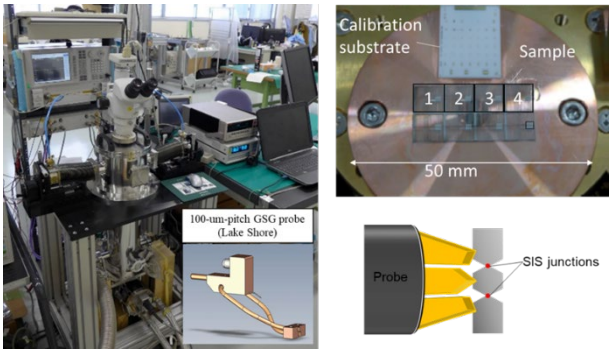

Fig. 4. Photographs of 4K probe station at NAOJ and device sample stage. The probe station allows to perform on-wafer characterization of SIS junction lots of various sizes at frequencies ranging from dc to microwave.

standards needed for 1-port Short-Open-Load, SOL calibration technique integrated right on the chip to be applied. This way, every measurement inherently includes fresh calibration in the same cooling cycle.

The dedicated test SIS wafer was designed and fabricated (Fig. 5). The test SIS wafer included single SIS junctions of different sizes for dc-IVC measurements (placed closely adjacent to the big external contact pads) and 112 test structures dedicated for capacitance characterization.

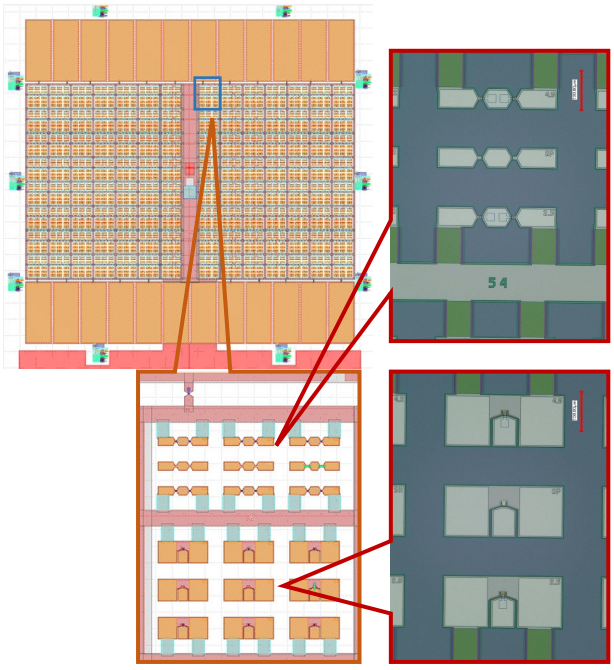

Fig. 5. The wafer (*upper left*) contains 112 test structures for capacitance characterization as well as single SIS junctions of different sizes for dc-IVC measurements (placed closely adjacent to the big external contact pads). Magnified view of the test structures (*lower left*) include structures with SIS junctions, as well as calibration patterns (open, short and load) – all for single and twin junctions' arrangements. Optical micrographs of fabricated structures are shown to the right

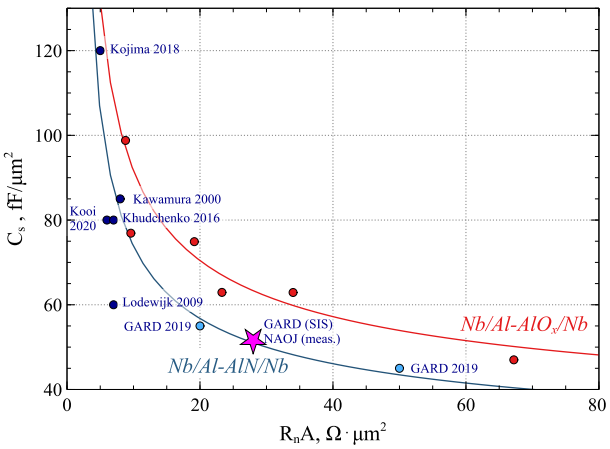

Fig. 6. Specific capacitance of Nb/Al-AlN/Nb junctions (*blue*) as compared with that of Nb/Al-AlO$_x$/Nb junctions [5] (*red*). The capacitance data for the junctions are approximated with semi-empirical relation $Cs = a / ln(R_n A)$ [7], where a is equal to 211 [5] for the Nb/Al-AlO$_x$/Nb junctions and to 170 for the measured Nb/Al-AlN/Nb junctions. The *dark-blue dots* are the data communicated by the other groups.

Each test chip contained structures with SIS junctions, single and twin junctions' arrangements, as well as standard patterns (open, short and load).

The measurement result (Fig. 6) has confirmed that specific capacitance of the Nb/Al-AlN/Nb junctions is noticeably lower than that reported for the Nb/AlO$_x$/Nb junctions, e.g. in [5], as well as the agreement between the measurements performed independently at GARD and at NAOJ is very good.

III. Conclusion

We have presented the status of SIS process developing capable of fabricating mixer chips for Next Generation ALMA receivers. The fabricated Nb/Al-AlN/Nb SIS junctions demonstrate excellent junction quality for the R$_n$A down to ~5 Ohm·μm^2 and down to submicron junctions' area defined by means of direct laser writing. Direct measurements of the Nb/Al-AlN/Nb SIS junctions' specific capacitance at GARD and NAOJ give the consistent results and confirm that the specific junction capacitance is ca. 20% lower than that for the Nb/Al-AlO$_x$/Nb junctions.

IV. Acknowledgement

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References

[1] J. Carpenter, et al., "The ALMA Development Program: Roadmap to 2030", *arXiv preprint arXiv:2001.11076. 2020,* Jan 29.

[2] A. Pavolotsky, et al., "Specific capacitance of Nb/Al-AlN/Nb superconducting tunnel junctions", *Proceedings of ISSTT 2019*, April 2019.

[3] P. Y. Aghdam, H. Rashid, A. Pavolotsky, V. Desmaris, D. Meledin, and V. Belitsky, "Direct Measurement of Superconducting Tunnel Junction Capacitance," *IEEE Trans. Terahertz Sci. Technol.*, 2015.

[4] T. Kojima, et al., "On-wafer capacitance Measurement of Nb-Based SIS Junctions with a 4-K Probe Station", *IEEE Transactions on Applied Superconductivity*, June 2017

[5] P.Y. Aghdam, et al., "Specific Capacitance Dependence on the Specific Resistance in Nb/Al–AlO$_x$/Nb Tunnel Junctions", *IEEE Transactions on Terahertz Science and Technology*, September 2017.

[6] T. Kojima, et al., "Contribution of Quantum Susceptance in SIS Junction Capacitance Measurement," *IEEE Trans. Appl. Supercond.*, 2019.

[7] V. Belitsky, et al., "100 GHz mixer with vertically integrated (stacked) SIS junction array," *Int. J. Infrared Millim. Waves*, 1993.