High-Efficiency Ka-Band Active Frequency Doubler MMIC in 150 nm GaN/SiC HEMT Technology

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***Abstract*—In this work, the design of an active single-balanced push-push frequency doubler Monolithic Microwave Integrated Circuit (MMIC) in 150 nm depletion mode GaN/SiC HEMT technology is discussed. The design yields a conversion gain of 7.6 dB with a half-power (3-dB) bandwidth spanning from 28.4 GHz up to 31.4 GHz for an input power of 15 dBm. On top of that, the maximum Power-Added Efficiency (PAE) is 10.2% and the harmonic rejection is larger than 27.4 dB at 30 GHz.**

***Index Terms*—Balanced Frequency Doubler, GaN HEMT Technology, High-Efficiency, Ka-Band, Marchand Balun, Monolithic Microwave Integrated Circuit (MMIC)**

I. Introduction

With the ever-increasing demand for higher data rates in communication systems, a shift to higher frequencies is needed. Specifically with the introduction of 5G Frequency Range 2 (FR2), spanning from 24 GHz up to 54 GHz, compared to 4G, being sub 6 GHz, hardware re-design is necessary. However, high-frequency Voltage-Controlled Oscillator (VCO) design with low phase noise and a wide tuning range is hard to achieve, so frequency multiplication will be critical to alleviate this issue [1].

Literature shows quite some research on frequency doublers in CMOS, SiGe, GaAs, and InP, whereas designs in GaN are rather scarce. In essence, the most appropriate design for a frequency doubler is the active single-balanced push-push topology, which inherently cancels out odd-order harmonic content due to anti-phase signaling, while even-order harmonic content is enhanced by superposition. This topology is often extended with a cascode to further boost the conversion gain and to minimize the Miller capacitance [2]–[4]. Another more uncommon way of increasing the conversion gain by eliminating the Miller capacitance is by adding cross-capacitive drain-gate neutralization [5]. As this design is optimized for high-efficiency and not for conversion gain, this has not been implemented.

This paper discusses the design methodology and measurement results of a high-power, high-efficiency active single-balanced push-push frequency doubler Monolithic Microwave Integrated Circuit (MMIC) in 150 nm depletion mode GaN/SiC HEMT technology, specifically in the Win Semiconductors NP15-00 process. The design has been made using the Keysight Advanced Designer Software (ADS) software. With an input power of 15 dBm at 15 GHz, this design provides an output power of 21.3 dBm, together with a Power-Added Efficiency (PAE) of 8.0% at 30 GHz. Moreover, the harmonic rejection is larger than 27.4 dB.

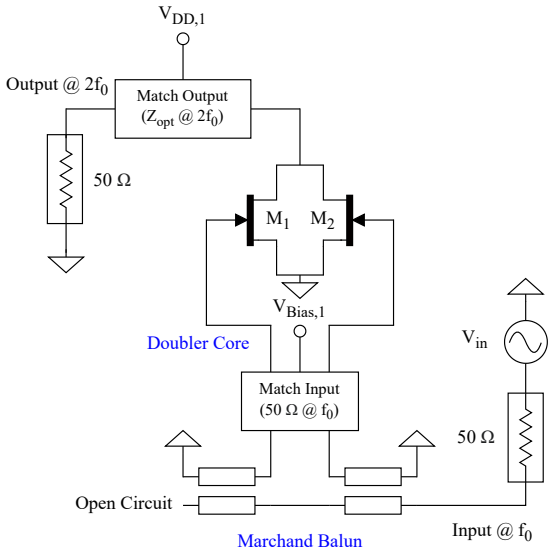

Fig. 1. Simplified schematic of the frequency doubler.

II. Design Methodology

Fig. 1 depicts the simplified schematic of the frequency doubler. The design of the core structure, matching networks, and Marchand balun will be discussed in more detail now. The full chip layout of the doubler is shown in Fig. 2 with dimensions 1.6 × 2.3 mm.

A. Marchand Balun Design

The first major challenge is the design of a compact balun functioning at 15 GHz. A Marchand balun can get bulky rather quickly as it is composed of half wavelength ($\lambda/2$) and quarter-wavelength ($\lambda/4$) transmission lines. Hence, a folded Marchand balun will reduce chip area for low-frequency designs. Fig. 2 presents the compactly folded Marchand balun at the bottom of the layout, where the inner half-wavelength conductor edge couples to the outer two quarter-wavelength

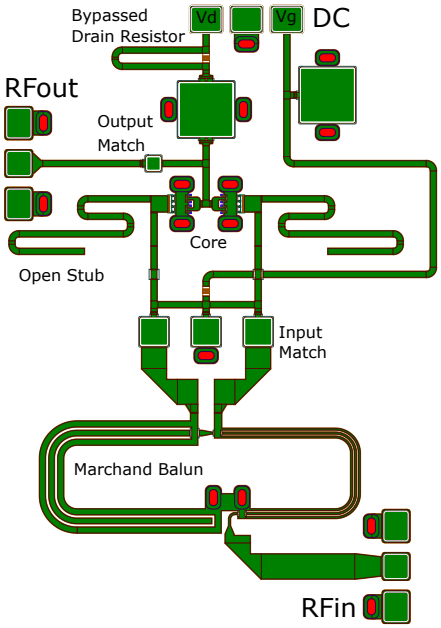

Fig. 2. Chip layout of the frequency doubler.

conductors [6]. The balun has a single-ended input impedance of 50 Ω and a differential output impedance of 100 Ω. The line impedances for the two branches of the balun have been optimized and have different values following the original Marchand balun paper [7]. Moreover, the phase imbalance is smaller than 3° and the structure only yields 0.8 dB loss in simulations. It is important to reduce the amplitude and phase imbalance as much as possible to improve the fundamental tone suppression.

B. Core Circuit Design

An active single-balanced push-push topology is employed, as the odd-order harmonics cancel out due to destructive anti-phases at the transistor drains, while the even-order harmonics add up constructively. The transistors are sized 4×50 μm to be able to carry a large output power of at least 20 dBm, while also being capable of producing some conversion gain. Increasing the transistor size further would increase the gate resistance, which is detrimental for the conversion gain. Lastly, the transistors are biased in class B to enhance the second order harmonic generation, as well as the efficiency. The gate bias is -2.7 V and the drain bias is 20 V.

C. Output Matching Network Design

The output matching network is designed to achieve the highest efficiency using harmonic load-pull, which yielded an optimum impedance of 5.1 + j27.2 Ω. A simple series-shunt transmission line pair is used to match to this value. Furthermore, at the top of the layout in Fig. 2, a large bypass capacitor can be seen at the drain line together with a bypassed drain resistor, which acts as a low-pass filter to prevent low-frequency instabilities in the circuit.

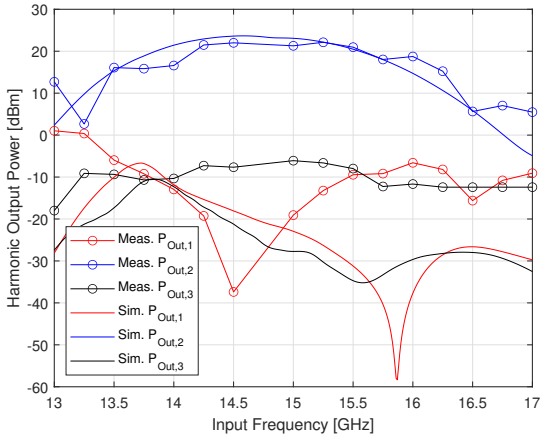

Fig. 3. Harmonic output power versus input frequency at an input power level of 15 dBm.

D. Input Matching Network Design

Having designed the output matching network, the input matching network is conjugately matched to 50 Ω using a simple series-shunt transmission line section. To prevent leakage of the second harmonic back to the transistor gates, a quarter-wavelength open stub is designed at the second harmonic frequency, being 30 GHz.

III. Measurement Results

The frequency doubler has been characterized using an Agilent E8257D signal generator and a Rohde&Schwarz FSUP-50 spectrum analyzer to properly capture all harmonic content. A power sweep has been performed to find the maximum PAE point at the desired center frequency of 30 GHz, finding an input power of 15 dBm. All presented results use this input power level.

Fig. 3 depicts the harmonic output power versus the input frequency for the first three harmonics. It can immediately be seen that the second harmonic is dominating significantly due to waveform superposition at the transistor drains, while the first and third harmonics are cancelled out. The measured harmonic rejection is 27.4 dB at an input frequency of 15 GHz. The simulated and measured data generally follow the same trend, while there are some discrepancies especially for the third harmonic, following from modeling errors of the non-linearities.

Fig. 4 shows the PAE and Conversion Gain (CG) of the proposed frequency doubler. The measurements yield a PAE of 8.0% at an input frequency of 15 GHz, and a maximum PAE of 10.2% at an input frequency of 15.5 GHz. Moreover, the design has a CG of 6.7 dB at an input frequency of 15 GHz, and a maximum CG of 7.6 dB at an input frequency of 14.3 GHz. Lastly, the half-power (3-dB) bandwidth of the second harmonic frequency of the doubler spans from 28.4 GHz up to 31.4 GHz, covering a total of 3.0 GHz.

TABLE I
COMPARISON TABLE OF PREVIOUSLY-DESIGNED FREQUENCY DOUBLERS.

	[8] (2002)	[9] (2004)	[10] (2007)	[11] (2010)	[1] (2019)	This Work
Technology [-]	SiGe HBT	90 nm SOI CMOS	150 nm GaAs	AlGaN/GaN	100 nm GaAs	150 nm GaN
Type [-]	Active	Active	Passive	Active - Hybrid	Active	Active
Topology [-]	Gilbert Cell	Single-Ended	Single-Balanced	Single-Ended	Single-Balanced	Single-Balanced
Frequency [GHz]	18 - 42	26.5 - 28.5	22 - 50	6.4 - 6.8	22 - 40	28.4 - 31.4
Conversion Gain [dB]	8.6	1.5	-12.5	14.8	-2	7.6
Harmonic Rejection [dB]	>22	>11	>19	>26	>38	>27.4
Output Power [dBm]	0	≈ -2	-	36.2	≈ 2.5	21.3
DC Power [mW]	185	10	0	32100	45	1326
PAE [%]	0.2	1.5	-	12.5	-	10.2
Chip Area [mm^2]	0.248	0.1	0.561	-	1.1	3.7

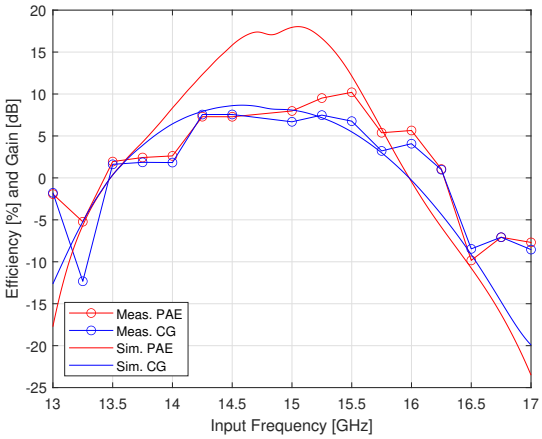

Fig. 4. Power-added efficiency and conversion gain versus input frequency at an input power level of 15 dBm.

IV. Discussion

Now, the frequency doubler proposed in this work is compared to other previous designs, as shown in Table I. It can be seen that the performance is very competitive in terms of conversion gain, harmonic rejection, and PAE. The bandwidth of the designed frequency doubler is rather limited, as there is an important trade-off between the achievable output power and bandwidth. Furthermore, there is no design in GaN technology for the desired frequency range, so therefore, a low-frequency hybrid GaN design is used in the comparison table [11]. It can be seen that this design also is optimized for a high output power and high PAE, as GaN technology is mainly used for power amplifier design. Since the input drive level is significantly higher for GaN designs, PAE is used as an efficiency calculation instead of conversion efficiency, as the input power is then taken into account. Following from the high output power, the DC power consumption is much higher compared to the other designs.

V. Conclusion

A high-power, high-efficiency active single-balanced push-push frequency doubler MMIC has been designed in 150 nm depletion mode GaN/SiC HEMT technology from 15 GHz to 30 GHz. The measurements results yield a maximum conversion gain of 7.6 dB and a half-power bandwidth from 28.4 GHz up to 31.4 GHz. Moreover, the design has been optimized for highest PAE, which is 10.2% at an input frequency of 15.5 GHz with an input power level of 15 dBm.

Acknowledgment

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References

[1] S. Chakraborty, L. E. Milner, S. Mahon, A. Parker, and M. Heimlich, "A GaAs frequency doubler with 38 dB fundamental rejection from 22 to 40 GHz using a transformer balun," *2019 49th European Microwave Conference (EuMC)*, pp. 848–851, 10 2019.

[2] J. J. Hung, T. M. Hancock, and G. M. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 754–761, 2 2005.

[3] N. Sarmah, K. Schmalz, W. Winkler, C. J. Scheytt, and S. Glisic, "122 GHz transmitter using frequency doublers," *2011 IEEE 11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 157–160, 2011.

[4] T. K. Johansen, A. S. Thualfiqar, N. Weimann, W. Heinrich, and V. Krozer, "Balanced G-band gm-boosted frequency doublers in transferred substrate InP hbt technology," *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 89–92, 12 2016.

[5] W. Lee and A. Valdes-Garcia, "W-band SiGe frequency doubler with optimum harmonic termination for 14% efficiency," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 3, pp. 272–275, 3 2021.

[6] M. Roberg and B. Kim, "A 6-12 GHz push-pull GaN amplifier for low harmonic drive applications," *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 12 2014.

[7] N. Marchand, "Transmission-line conversion," *Electronics*, vol. 17, pp. 142–145, 1944.

[8] S. Hackl and J. Böck, "42 GHz active frequency doubler in SiGe bipolar technology," *2002 3rd International Conference on Microwave and Millimeter Wave Technology, 2002. Proceedings. ICMMT 2002*, pp. 54–57, 2002.

[9] F. Ellinger and H. Jäckel, "Ultracompact SOI CMOS frequency doubler for low power applications at 26.5-28.5 GHz," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 2, pp. 53–55, 2 2004.

[10] C. S. Lin, P. S. Wu, M. C. Yeh, J. S. Fu, H. Y. Chang, K. Y. Lin, and H. Wang, "Analysis of multiconductor coupled-line marchand baluns for miniature mmic design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 6, pp. 1190–1198, 6 2007.

[11] K. Yuk, G. R. Branner, and C. Wong, "High power, high conversion gain frequency doublers using SiC mesfets and AlGaN/GaN hemts," *2010 IEEE MTT-S International Microwave Symposium*, pp. 1008–1011, 2010.