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# Gate Pulsing as a Transient Ringing Reduction Method for Multi-Level Supply Modulators

Connor Nogales, Zoya Popović, Gregor Lasser

***Abstract*—This letter demonstrates a gate pulsing technique to reduce the ringing in multi-level dynamic voltage supplies used for modulating the drain bias of GaN radio-frequency power amplifiers (RFPAs). Supply modulation can improve overall average efficiency when the RFPA is amplifying signals with varying envelopes. Multi-level discrete supply modulators (SMs) are used for high instantaneous bandwidth signals when continuous modulators become inefficient. These SMs provide several voltage levels to the RFPA using transistor switches. By pulsing the gate drive of switches on and off quickly before ultimately turning them on, the switches undergo an intermediate lossy state which reduces the ringing. The pulse settings can be individually adjusted for different voltage level transitions and loads. Gate pulsing is compared to conventional ringing reduction techniques such as varying the fixed series gate resistance, and dead-time optimization. Gate pulsing experimental results with a 4-level SM and 8 MHz 64-QAM signal show a significant improvement in ringing over dead-time optimization with only a 0.9% points drop in efficiency.**

***Index Terms*—Envelope tracking, Multi-Level Converter, Power Amplifier, Ringing, Supply Modulation.**

## I. Introduction

Supply modulation, also known as envelope tracking, is an RFPA efficiency enhancement method where the drain voltage of the RFPA is dynamically varied according to the input signal envelope [1]. A challenge in this technique is the design of a dynamic voltage supply (supply modulator) capable of efficiently producing a high slew-rate and high output power signal with low distortion. Continuous supply modulators such as buck converters have been used extensively, however suffer from reduced efficiency when tracking high bandwidth signals [1]. Discrete supply modulation, which switches between dc voltage levels, demonstrated tracking high bandwidth signals by minimizing the number of switching instances to maintain high efficiency, with switching in the 100-MHz range [2], [3]. The discrete supply modulator architecture used in this work is a multi-level converter with transistor switches that apply the different externally generated dc voltage levels at the output, $V_{\text{out}}$, as shown in Fig. 1a. A challenge of this architecture is that upon each voltage level transition, there is undesired ringing in the output voltage applied to the RFPA (Fig. 1b). This ringing creates spurious mixing products in the nonlinear RFPA which degrades linearity metrics such as error vector magnitude and adjacent channel power ratio [4]–[6], in addition to limiting the maximum switching speed of the converter [7]. Therefore, minimizing the output voltage ringing is a critical aspect of discrete supply modulator design.

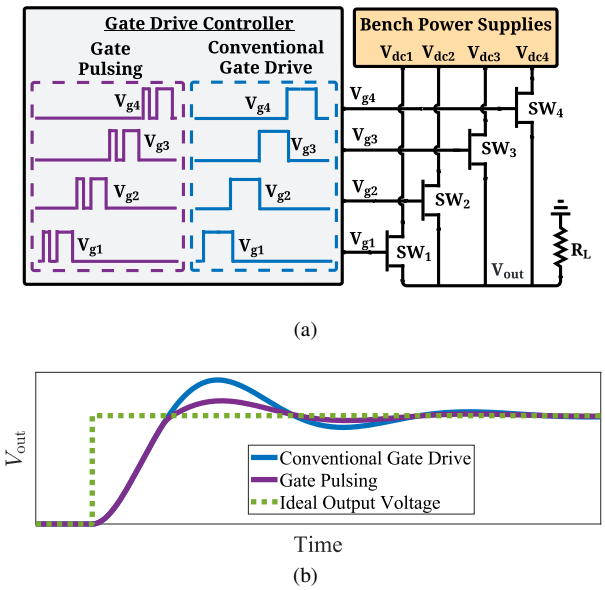


Fig. 1. (a) Schematic and gate drive signals of the high power multi-level converter (b) Example of output voltage ringing comparing the conventional gate drive, gate pulsing, and the ideal cases.

In typical power converter designs, the reduction of electromagnetic interference (EMI) created by fast switching transients is an important topic [8]. For supply modulator designs, the output voltage ringing itself is more important than EMI issues, however the two topics are closely related. There are several methods employed in the literature to reduce EMI that occurs during switching transients. Techniques that actively control the switch slew rate are known as active gate drive topologies [9]. Among these are variable gate resistance [10], variable gate current [11], and variable gate voltage circuits [12], [13]. In addition, the dead-time (DT) can also be adaptively optimized to improve efficiency [14] or reduce EMI [15]. These components are typically feedback controlled through a sensing circuit and dedicated digital control circuitry. This makes the switched supply reconfigurable under changing load conditions, however, the approach is difficult to implement and significantly increases complexity and cost. Ringing can also be reduced through the use of a resonant filter or snubber network, however, a filter reduces the bandwidth, while a snubber network decreases the converter efficiency.

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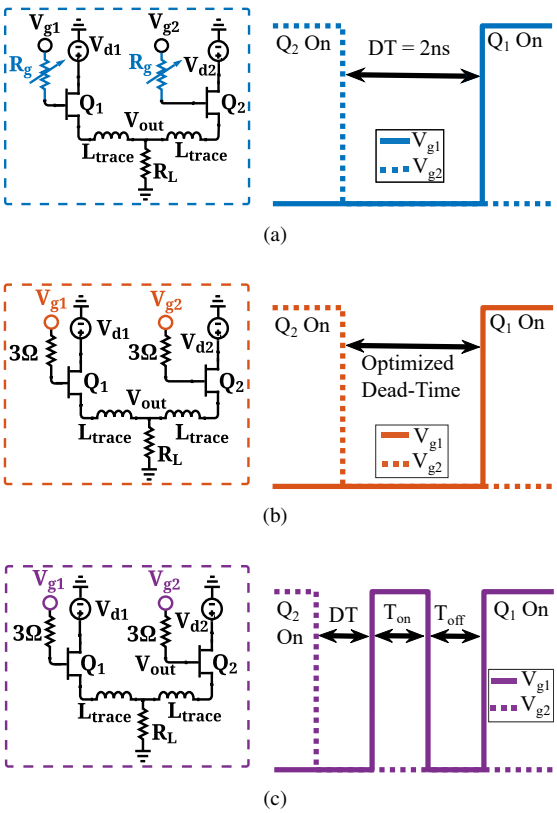


Fig. 2. Two-level schematics and idealized gate drive signals of the three ringing reduction techniques compared in this work: (a) increased gate resistances (3 – 10 Ω) with a fixed dead-time; (b) dead-time optimization; and (c) gate pulsing.

This letter presents a new pulsed-gate ringing reduction technique compatible with multi-level converter architectures. The technique is compared with two conventional approaches: increasing fixed series gate resistance; and DT optimization. The corresponding schematic and idealized gate drive signals are shown in Fig. 2a-c. The gate pulsing technique does not require any additional hardware, is reconfigurable for different loads, and reduces the ringing beyond what increasing gate resistance and DT optimization are capable of, without compromising efficiency. For the comparison, different techniques are applied to a high power (800 W) multi-level converter (HPMLC) while tracking the envelope of an 8 MHz 64–QAM signal.

## II. Supply Modulator Test Setup

The HPMLC used in this work is presented in [7] and switches between four evenly spaced externally generated dc voltages of 10, 13.3, 16.7, and 20 V. A schematic of the converter is shown in Fig. 1a. Each switching cell consists of two commercially available E-mode GaN HEMT transistors (GS61008T) in parallel. The input signal is generated from a bit pattern generator (BPG) with multiple synchronous channels. For each individual switching cell the input signal is logic level converted through a comparator and then amplified through an isolated gate driver (UCC21520ADW) which drives the E-mode GaN transistor gates to 5 V above their respective dc voltage levels with a typical rise/fall time of 6/7 ns. A fixed surface mount resistor $R_g$ in series with each of the transistor gates limits the gate current during switching transients and prevents damage to the gate drivers.

The converter is evaluated using an 8 MHz 64–QAM signal envelope transmitting 5 MS/s with a root-raised cosine filter and a roll-off factor of 0.25. The signal envelope is translated into a discretized four-level signal through a shaping function that relates the instantaneous RFPA modulated signal input power to a particular drain voltage [1], [7]. The maximum switching speed of the discrete output signal is 10 MHz corresponding to a minimum pulse width of 100 ns. The output voltage and current are measured using an oscilloscope as in [7]. The output power is determined by multiplying the current and voltage waveforms and integrating across the signal duration. The input power is calculated by summing the power supplied from each of the dc supplies and the efficiency is the ratio of the output and input power. The ringing in the measured signal is evaluated by the root mean square error (RMSE), given by:

$$RMSE = \sqrt{\frac{\sum_{i=1}^{N} \left(V_{\text{meas.}}(i) - V_{\text{ideal}}(i)\right)^2}{N}}, \qquad (1)$$

where $N$ is the number of measured points over the entire duration of the signal, $V_{\text{meas.}}$ is the measured waveform, and $V_{\text{ideal}}$ is the desired discrete output signal with perfectly sharp transitions and no ringing. The dc levels of the ideal signal are shifted to account for ohmic losses in the transistor.

## III. Ringing Reduction Comparison

### A. Gate Resistance Study

Increasing the series gate resistance of each GaN transistor switch can potentially reduce the ringing through a decrease in slew rate. In order to investigate this, the HPMLC is evaluated with fixed series gate resistance values of 3, 5, and 10 Ω, across nine load resistances ranging from 20 to 0.4 Ω. The efficiency and RMSE of the HPMLC while tracking the 8 MHz 64–QAM signal is shown in Fig. 3 for the three different gate resistances. For low average power levels below 50 W a gate resistance of 3 Ω results in the lowest RMSE. For medium power levels between 50 W and 150 W the 5 Ω case is best. For high power levels exceeding 150 W the 10 Ω case results in the best RMSE with a small cost to efficiency. From this investigation, it is evident that the optimal series gate resistance is load dependent. For systems with varying loads, e.g. dynamically driven PAs, an adaptable ringing reduction method is required.

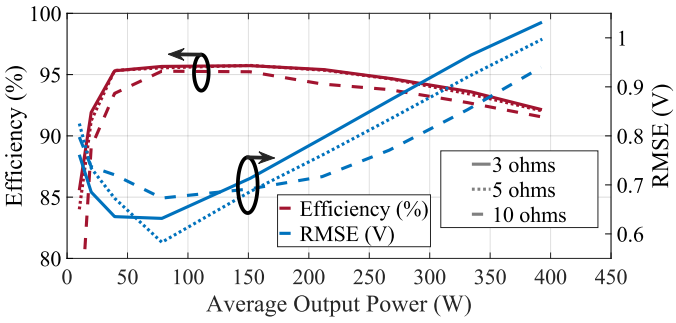


Fig. 3. Converter efficiency and RMSE while tracking an 8 MHz 64–QAM signal with three different series gate resistances.

### B. Gate Pulsing and Dead-Time Optimization

In order to reduce the ringing that occurs upon each upward transition, the gate of each switch being turned on was pulsed on and off before reaching its final on-state as shown in Fig 2c. For this technique to be successful, the pulse parameters $T_{\text{on}}$, $T_{\text{off}}$, and the DT settings must be tuned for each of the six individual voltage transitions. This is necessary to account for variations in the different switches and gate drivers. For instance, varying rise/fall times, threshold voltages, and propagation delays can effect the optimal pulse parameters. Gate pulsing was first investigated in the time domain simulator LTspice with a transistor model provided by the manufacturer and the parasitics from the gate trace and transistor interconnect modeled as $RLC$ circuits. This simulation model is validated with measurement data in [7].

The simulated gate and output voltages of the two parallel transistors connected to the 13.3 V level are shown in Fig. 4 with and without gate pulsing for the 10 to 13.3 V transition. When the gate is pulsed, the transistors goes into a lossy state while switching on. As the output voltage rises, the oscillating energy stored in the reactive elements of the transistors and output trace is converted to heat by the transistor resistance thus the output voltage ringing is dampened. The dissipated power in the transistors is plotted as a function of time in Fig. 4. With gate pulsing the average dissipated power from 0 to 70 ns increases from 0.85 to 1.02 W and the total steady-state power delivered to the load is 35.2 W. These simulations illustrate how the gate pulsing technique can significantly reduce output voltage ringing with only a minimal increase in dissipated power.

In order to obtain the optimal pulse and DT settings in measurements, a continuously repeated test signal is used which switches between each of the voltage levels with an equal duty cycle and remains at each voltage level for 10 µs. With this signal, pulse settings $T_{\text{on}}$, $T_{\text{off}}$, and DT are swept for each upward transition and applied only to switches being turned on. At each optimization setting, the ringing is compared to a reference case that has 2 ns of DT, a gate resistance of 3 Ω, and no gate pulsing. For each setting, the output voltage is measured and the RMSE is calculated over a short window that starts when the reference case output

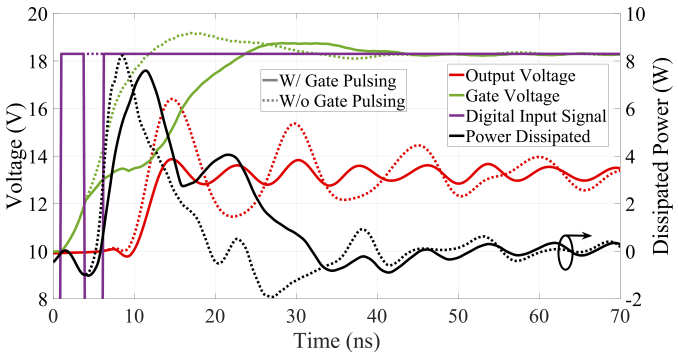


Fig. 4. Simulated output voltage, gate voltage, digital input signal, and power dissipated in the transistor switch for the 10 to 13.3 V transition with and without gate pulsing.

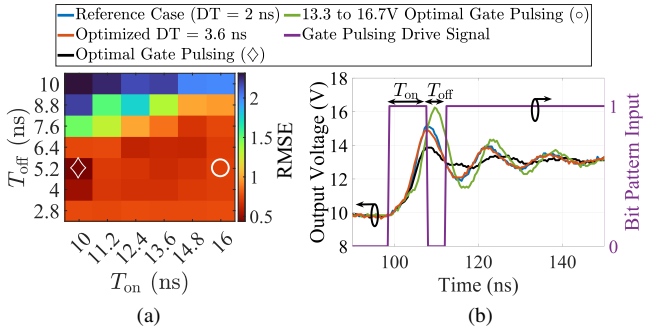


Fig. 5. Gate pulsing results of the 10 to 13.3 V transition. (a) NRMSE over the gate pulse parameters sweep with a DT of 3.6 ns and (b) time domain waveforms.

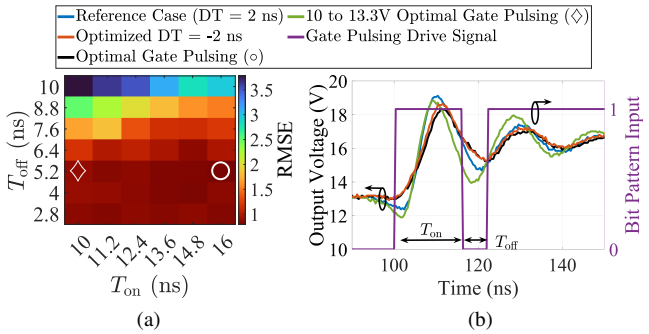


Fig. 6. Gate pulsing results of the 13 to 16.7 V transition. (a) NRMSE over the gate pulse parameters sweep with a DT of −2 ns and (b) time domain waveforms.

voltage initially crosses its steady-state dc voltage at the higher level and ends when the waveform settles. The RMSE at each pulse setting is normalized to the RMSE of the reference case and referred to as the normalized root mean square error (NRMSE). Values less than one indicate an improvement through DT optimization or the gate pulsing technique over the reference case. A coarse sweep of the three pulse parameters ($T_{\text{on}}$, $T_{\text{off}}$, and DT) is measured with $T_{\text{on}}$ and $T_{\text{off}}$ swept in 1.2 ns steps and DT swept in 0.4 ns steps. After an optimal region of the coarse sweep is selected, the DT is fixed and the ($T_{\text{on}}$) and ($T_{\text{off}}$) values are swept at the finest resolution of the BPG (0.4 ns).

The NRMSE of the coarse sweeps of the 10 to 13.3 V and 13.3 to 16.7 V are shown in Figures 5a and 6a as a function of the gate pulse settings $T_{\text{on}}$ and $T_{\text{off}}$ for a fixed optimal DT with a load of 5 Ω. The two markers indicate the optimal $T_{\text{on}}$ and $T_{\text{off}}$ settings over the coarse sweep for the 10 to 13.3 V (♢) and 13.3 to 16.7 V (○) transitions. The corresponding time domain waveforms are shown in Figures 5b and 6b. From these plots, we can see that the gate pulsing can yield significant improvements in ringing over DT optimization. Furthermore, if optimal settings for one transition are applied to another, then the advantage from gate pulsing can be lost as is the case in Fig. 6b or can add even more ringing as is the case in Fig. 5b. The optimal settings for each of the six transitions are shown in Table I for a 5 Ω load resistance. For each transition, the NRMSE can be improved beyond the DT optimization results through the use of gate pulsing.

The optimal gate pulsing and DT optimization parameters

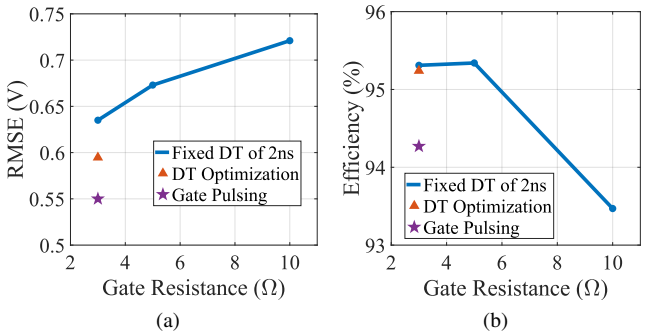


Fig. 7. (a) RMSE and (b) efficiency vs series gate resistance at a load of 5 Ω while tracking an 8 MHz 64–QAM signal.

were implemented in a look-up table and applied to the HPMLC while tracking the envelope of the previously described 8 MHz 64–QAM signal at a load resistance of 5 Ω. The resulting converter RMSE and efficiency when using the gate pulsing and DT optimization techniques are compared to fixed gate resistances of 3, 5, and 10 Ω with 2 ns of DT in Fig. 7. The reference case of fixed DT without gate pulsing and a gate resistance of 3 Ω yields a RMSE of 0.63 V. Through DT optimization the RMSE is reduced to 0.59 V and through gate pulsing the RMSE is reduced further to 0.55 V with only a 0.9% points cost to efficiency while tracking the 64–QAM signal. The ringing creates additional spectral content between 30 and 80 MHz as shown in Fig 8. Through gate pulsing, this spectral content can be attenuated, thus moving closer to the ideal drain signal case.

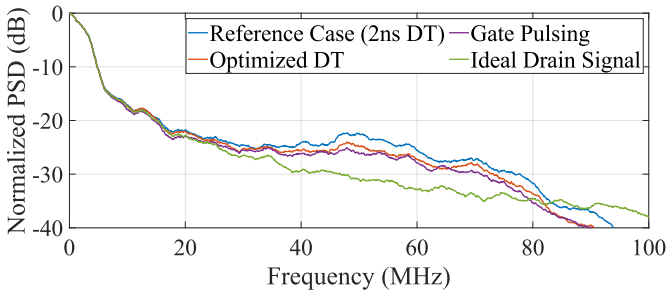


Fig. 8. Frequency spectrum comparison of the reference case, optimized dead time, gate pulsing method, and ideal drain voltage waveforms while tracking the 8 MHz 64 QAM signal each with a gate resistance of 3 Ω.

TABLE I
IMPLEMENTED PULSE SETTINGS, DT, AND NRMSE FOR THE DT OPTIMIZATION AND GATE PULSING TECHNIQUES WITH A 5 Ω LOAD.

| | DT Opt. | | Gate Pulsing | | | |
|---|---|---|---|---|---|---|
| **Transition** | $DT_{\text{opt}}$ **(ns)** | **NRMSE** | $T_{\text{on}}$ **(ns)** | $T_{\text{off}}$ **(ns)** | $DT$ **(ns)** | **NRMSE** |
| 10-13.3 V | 3.6 | 0.88 | 9.2 | 4.4 | 3.6 | 0.39 |
| 10-16.7 V | 5.2 | 0.76 | 10 | 6 | 6 | 0.66 |
| 10-20 V | 6 | 0.50 | 10 | 5.2 | 6 | 0.30 |
| 13.3-16.7 V | -2 | 0.75 | 16 | 6 | -2 | 0.68 |
| 13.3-20 V | -0.8 | 0.84 | 10.4 | 4.8 | -0.8 | 0.59 |
| 16.7-20 V | -2 | 0.76 | 10.4 | 4.4 | 0 | 0.63 |

## CONCLUSION

A new ringing reduction technique for multi-level supply modulators is experimentally validated. This gate pulsing technique does not require any additional circuitry and is flexible such that the pulse timing for individual voltage transitions and different power levels can be individually optimized. Gate pulsing reduces the ringing beyond what dead-time and variable gate resistance is capable of with only a small drop in efficiency. This technique is applied to a 800 W multi-level converter while tracking the envelope of an 8 MHz 64–QAM signal. When compared to a reference case with conventional gate driving and a gate resistance of 3 Ω the RMSE is improved by 12.7% with only 0.9% points cost to efficiency when using gate pulsing on each upward transition. The improvement in RMSE reduces in-band and out-of-band distortion created by the supply modulator in an efficient envelope-tracked wireless transmitter.

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