A 10-W6-12GHz GaN MMIC Supply Modulated Power Amplifier

A 10-W 6–12 GHz GaN MMIC Supply Modulated Power Amplifier

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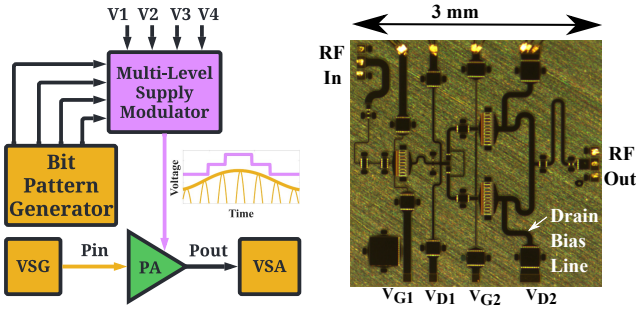
***Abstract*— This paper presents a gallium nitride (GaN) Monolithic Microwave Integrated Circuit (MMIC) PA with octave bandwidth, designed specifically for amplifying high peak-to-average power ratio (PAPR) signals with high efficiency from 6 to 12 GHz. Across the octave bandwidth, greater than 23.0% PAE is achievable over 10-dB of back off power using a dynamic supply voltage range from 6 to 20 V. We present the design and CW characterization of the PA as well as measurements using a 10-MHz multi-carrier noise-like signal and a 4-level discrete supply modulator comparing four different tracking functions. At 6.5 GHz a flat-gain, uniform voltage spacing function yields a 2.5 dB improvement in noise power ratio (NPR) over the static 20 V results with 3.8% points of PAE improvement, reaching 35.0 dBm of average output power. Furthermore, for a target NPR of 20 dB supply modulation yields a 9.7,% point improvement in PAE over the static case with a 1.5 dB increased output power.**

***Keywords*— Power amplifier, MMIC, GaN, octave bandwidth, supply modulation**

I. Introduction

Modern RF and microwave systems demand efficient power amplifiers (PAs) for challenging wide-band signals with high PAPR in communication and electronic warfare applications. Octave bandwidth designs capable of achiving high back-off efficiency were recently reported both for Doherty amplifiers [1] and load modulated balanced PAs [2], but these topologies require the combination of multiple RF amplifiers which necessitates a large chip area when integrated on a MMIC. Other broadband PA design techniques such as push-pull [3], balanced [4], and reactively combined PAs [5] achieve the required bandwidth but have low back-off efficiency. Back-off efficiency can however be substantially improved through the use of supply modulation (SM), where the drain voltage of the PA is dynamically modulated according to the instantaneous output power. In addition SM not only provides efficiency enhancement in back-off, but can also be used to control the gain of a PA and improve linearity [6].

This paper describes a two stage GaN MMIC PA specifically designed for SM from 6 to 12 GHz with a target peak output power of 40 dBm. The device selection, load pull data and stability considerations are reported first, followed by a discussion of the continuous wave (CW) small and large signal measurement results for various static drain voltages. Finally, the PA is characterized under dynamic SM conditions using a 10 MHz noise-like signal at 6.5 GHz and the resulting linearity and composite efficiency for different shaping functions are compared to static drain voltages.



(a) (b)

Fig. 1. (a) Block diagram of a dynamically supply modulated PA and (b) Photograph of the 10W 6-12 GHz MMIC PA.

II. Foundry and Device Selection

The two stage MMIC PA described in this paper was fabricated in the WIN Semiconductors' NP15 GaN on SiC process. The process utilizes 150 nm gate lengths, a power density of 5.4 W/mm at 29 GHz [7], and a transit frequency f_t of 35 GHz. Fig. 1b shows the MMIC PA with an overall size of 3 ×3 mm. It consists of two 20×100 μm devices in the final stage with a single 16×100 μm driver in the first stage (staging ratio of 1:2.5). The large device sizes were chosen to minimize the combining structure while achieving the targeted output power of 10 W from 6 to 12 GHz. Each device utilizes outside source vias in order to make the transistor size more compact and is biased at 125 mA/mm at a nominal drain voltage of 20 V.

III. Load Pull and Matching Network Design

The PA design is tailored for the drain to be supply modulated when amplifying signals with a high PAPR. Simulated load-pull contours of a single 20×100 μm device at 9 GHz is shown in Fig. 2a at drain voltages of 10, 15, and 20 V. Each contour plotted in 5% steps referenced to the maximum PAE of 69.8%, 70.0%, and 69.3% at 10, 15, and 20 V respectively. The optimal load impedance rotates clockwise with increasing voltage primarily due to the decreasing drain-source capacitance in the transistor.

The statistics of a signal with a high PAPR dictate that the PA operates more often at backed-off power levels, which correspond to medium and low drain voltages when applying dynamic SM. Therefore in order to optimize the average efficiency, this PA is designed for peak efficiency at 15 V. The

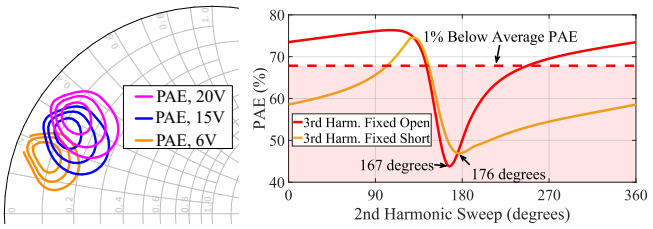


Fig. 2. (a) 9 GHz load pull of 20×100 μm device at drain voltages of 6, 15, and 20 V each with a maximum PAE of 69.8%, 70.0%, and 69.3% respectively in 5% contour steps referenced to the maximum PAE at the center of each contour. (b) Sweep of the 2$^{\text{nd}}$ harmonic phase when the 3$^{\text{rd}}$ harmonic is fixed with an open and short at an f_0 of 6 GHz.

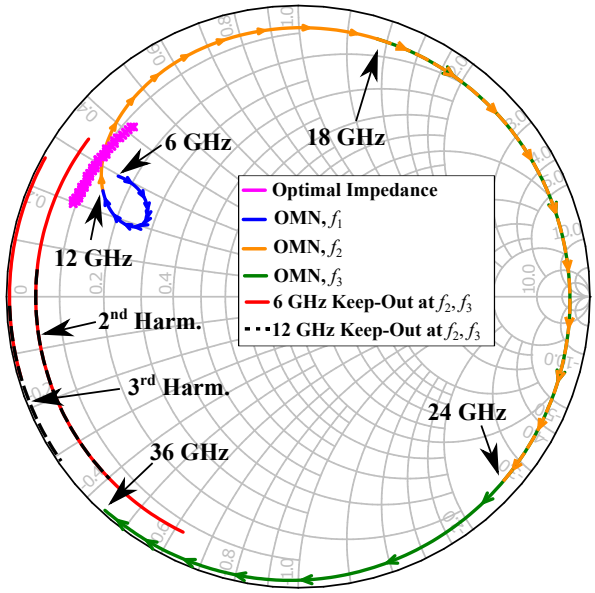


Fig. 3. Efficiency-optimal fundamental loadpull impedance for the final stage device at 15 V, compared to the implemented fundamental, 2$^{\text{nd}}$, and 3$^{\text{rd}}$ harmonic impedances and corresponding keep out regions at the band edges as defined in Fig. 2b.

maximum PAE load impedance at 15 V and 9 GHz is converted to an equivalent parallel RC circuit and used to design the output matching network (OMN) across the octave bandwidth. The input of the devices are conjugately matched at 15 V.

Load pull of the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ harmonics reveals that poor termination at harmonic frequencies can result in a significant drop in efficiency [5]. Fig. 2b as an example shows a sweep of the 2$^{\text{nd}}$ harmonic phase with the 3$^{\text{rd}}$ harmonic open circuited and shorted at 6 GHz. In both cases a short circuit of the 2$^{\text{nd}}$ harmonic results in a PAE drop of over 30% from the peak value. Using load pull data for 2$^{\text{nd}}$ and 3$^{\text{rd}}$ harmonic sweeps, a keep-out region is defined where the termination angle results in a PAE drop 1% below the average PAE across all sweep angles. The keep-out regions are shown in Fig 2b indicated as angles where the PAE is below the dotted line.

The PAE-optimized load-pull impedances of the 20×100 μm device are shown in Fig. 3 from 6 to 12 GHz when the input is conjugate-matched at 9 GHz and the PA is driven at 26 dBm of input power. These ideal impedances are compared to the OMN impedance from 6 to 36 GHz along with the keep-out regions for the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ harmonics at 6 and 12 GHz. For each load pull simulation, the harmonics not being swept are set to a fixed open circuit with a magnitude of 0.95. The magnitude of the 2$^{\text{nd}}$ harmonic keep-out region is slightly reduced for visual clarity. The keep-out regions are mostly avoided, except at the 2$^{\text{nd}}$ harmonic of 6 GHz which falls into the octave bandwidth and the fundamental match at 12 GHz is prioritized.

Each matching network is synthesized using series and shunt transmission lines and capacitors. The gate and drain bias lines are incorporated into the matching networks as shunt transmission line sections. This allows for tight control of the bias line impedance over the entire octave bandwidth and enhances the in-band stability. Furthermore, by avoiding the use of large inductive chokes on the drain bias lines and minimizing the drain bypass capacitance, the bandwidth of the supply modulator to PA interconnect is increased, thus enabling higher switching speeds.

The small input impedance of the large devices makes it challenging to achieve a broadband impedance match at the input and inter-stage. For instance, the input impedance of the 16×100 μm driving device at 9 GHz is Z_{in}= 0.33 - j2.2 Ω when loaded by the inter-stage matching network and final stage. In order to make the input impedance more manageable, a series 1.3 Ω resistance is added to the gate of the first stage using a thin film resistor available in the process. This improves the return loss and stability at the expense of gain and PAE. Stability resistors of 1.6 Ω and 13 Ω are added in series with the first and second stage gate bias lines close to the bypass capacitors. 50 Ω resistors are placed across the two branches in the inter-stage matching network to suppress odd-mode instabilities. Finally the stability of the PA is evaluated using the Nyquist criterion from 1 MHz to 36 GHz at drain voltages from 10 to 20 V in 1 V steps.

IV. PA CW Characterization

In order to perform CW measurements of the PA, the MMIC was mounted on a copper molybdenum slab along with 100 pF and 1000 pF off-chip bypass capacitors placed in parallel with each of the gate and drain bias lines.

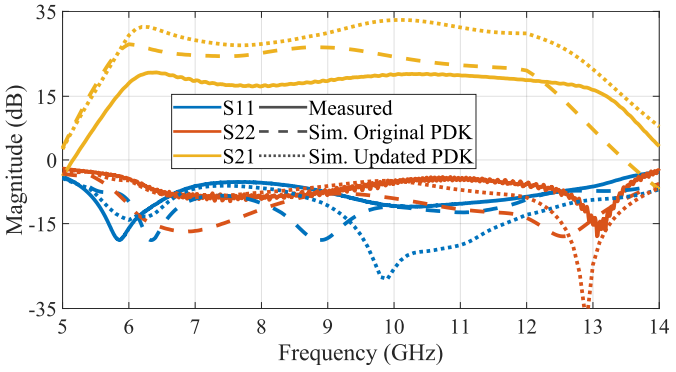


Fig. 4. Measured magnitude of scattering parameters of the PA compared to simulated results using two different PDKs at a drain voltage of 20 V.

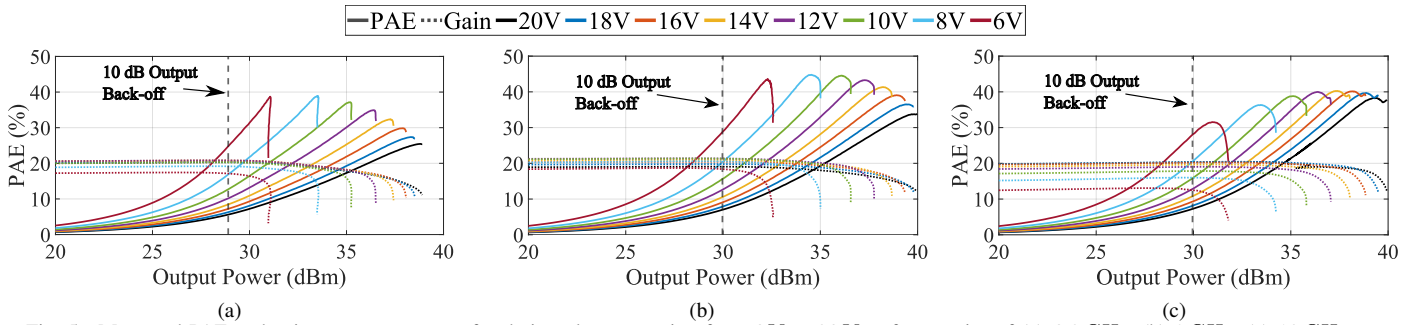


Fig. 5. Measured PAE and gain vs. output power for drain voltages ranging from 6 V to 20 V at frequencies of (a) 6.3 GHz, (b) 9 GHz, (c) 12 GHz.

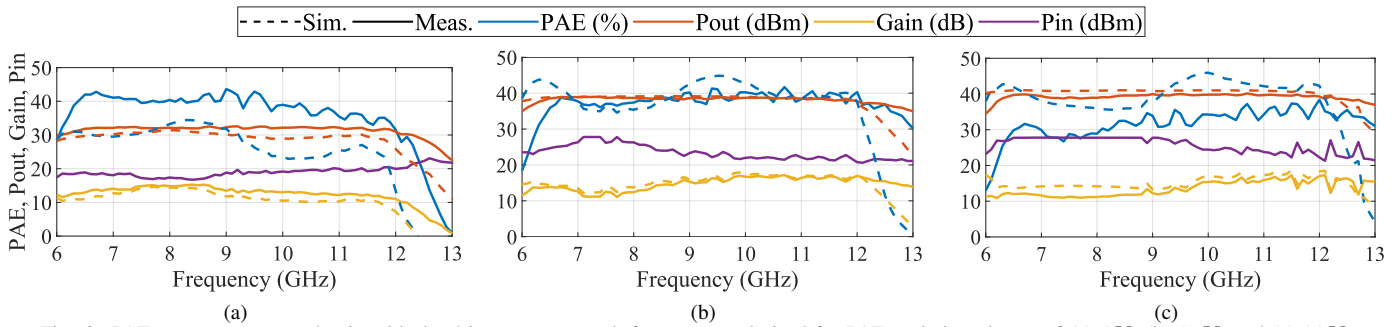


Fig. 6. PAE, output power, and gain with the drive power at each frequency optimized for PAE at drain voltages of (a) 6 V, (b) 15 V, and (c) 20 V.

The off-chip drain capacitance helps ensure stability during on-wafer probing and are omitted when the PA is supply modulated. The measured and simulated S-parameters of the PA are shown in Fig. 4 at a drain voltage of 20 V. In measurements, the small and large signal characteristics are slightly shifted towards higher frequencies, covering 6.3 to 12.6 GHz. The simulations use the PDK model that the MMIC was designed with, as well as an updated model provided after tape-out. The measured $|S_{21}|$ of the PA is slightly lower than what was simulated and varies from 17.3 to 20.5 dB while the return loss is better than 5 dB across the band. The updated PDK model more accurately predicts $|S_{11}|$ and $|S_{22}|$ as well as the shifted bandwidth, however, $|S_{21}|$ is significantly larger across the band.

The CW large signal PAE and gain are shown in Fig. 5a – c as a function of output power for drain voltages from 6 to 20 V with 2 V spacing, at 6.3, 9, and 12 GHz. Across a 10 dB back-off range utilizing drain voltages from 6 to 20 V, the PAE is greater than 24.9%, 28.8%, and 28.2% at 6.3 GHz, 9 GHz, and 12 GHz. In addition, we observe a backed-off gain variation of 3.4 dB, 2.7 dB and 7.3 dB respectively, at these same frequencies. The lower gain variation found at low and medium frequencies reduces the linearity degradation of the PA when it is supply modulated. The large signal frequency dependence of the PAE, gain, input power and output power is shown in Fig. 6a-c. For each frequency point the drive power is chosen for maximum PAE at the corresponding drain voltage. The dashed lines show the simulated results using the original PDK model and the same input powers. When the input power is optimized for PAE a very flat output power response is observed for all drain voltages. At 20 V the output power exceeds 39.5 dBm from 8.4 to 11.6 GHz, and the power exceeds 38.1 dBm across the full 6.3 to 12.6 GHz bandwidth.

V. Supply Modulation Results

The PA is supply modulated using a four-level MMIC discrete drain supply modulator (DSM) described in [8] and a 10 MHz noise-like multi-carrier signal with a PAPR of 10.6 dB and 5% spectral notch in the center. Spectral regrowth in the notch is a result of inter-modulation between the carries and distortion caused by discrete switching of the supply. The ratio between the in-band average power outside the notch and the average power in the notch is a measurement called noise power ratio (NPR) which is used to evaluate the linearity of the PA. The baseband signal is applied through a vector signal generator and external driver. Couplers on the input and output are used to measure the power and spectrum.

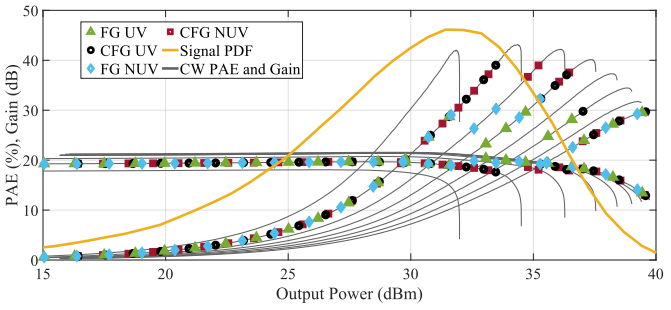
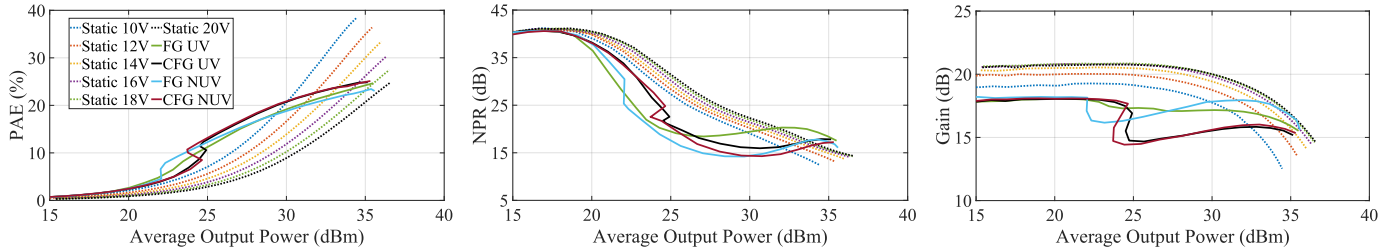


Fig. 7. Discrete tracking functions at 6.5 GHz plotted over CW measurements of PA from 6 to 20 V in 2 V steps. FG UV: SF optimized for flat gain with uniform step-voltage spacing; CFG UV: SF optimized for compressed flat gain with uniform spacing; FG NUV and CFG NUV: SFs for the two cases with non-uniform drain voltage step spacing.

A look-up shaping function (SF) between the instantaneous output power and drain supply voltage is generated from



(a) (b) (c)

Fig. 8. Measured (a) composite PAE, (b) NPR, and (c) gain vs. average output power with different shaping functions for a 10 MHz noise-like signal at 6.5 GHz. The dynamic supply modulated results are compared to the static drain voltage case.

measured CW PAE, gain and output power. The SF and discrete voltage spacing can be tailored for maximum PAE, flat gain or any other PA metric with a drain voltage dependence [6], [9]. The four SFs used in this work are plotted in Fig. 7 at 6.5 GHz along with the static CW PAE, gain, and signal probability density function. The first SF is a flat-gain (FG) trajectory with uniform voltage spacing (UV) of 8, 12, 16, and 20 V. The second is a compressed flat-gain (CFG) trajectory with uniform voltage (UV) spacing which still aims at a flat gain but allows for 1.5 dB of PA compression. Since the gain variation is larger at the lower drain voltages, a non-uniform voltage spacing (NUV) is utilized in order to get a more even distribution of the gain variation. The NUV spacing uses voltages of 8, 10, 12, and 20 V. The flat-gain and compressed flat-gain SFs are applied to the NUV spacing in the third and fourth trajectories. In order to further reduce the gain variation, the lowest voltage was chosen to be 8 V rather than 6 V. This improves the NPR with only a minimal drop in PAE.

The measured dynamically supply modulated PAE, NPR, and gain are plotted vs. output power in Fig 8 at 6.5 GHz where they are compared to static drain voltages from 10 to 20 V in 2 V steps. The PAE of the supply modulated amplifier includes losses in the DSM, de-embedded from the static drain voltage results. At an output power of 23 dBm the DSM begins switching to the highest voltage level of 20 V. At this power we observe a steep drop in gain which is possibly caused by memory effects in the PA due to the dynamic switching. This phenomenon is not observed at higher power levels. At 6.5 GHz the FG UV trajectory improves the NPR by 2.5 dB with 3.8 percentage points (pp) higher PAE as compared to the 20 V static case at an output power of 35.0 dBm. Furthermore, for a target NPR of 20.0 dB the PAE is improved by 5.5 and 9.7 pp. with 4.5 dB and 1.5 dB greater output power over the 10 and 20 V case. The compressed flat-gain SF yield the highest PAE with a lower NPR than the flat-gain SFs with the same voltage spacing. The UV produces a higher NPR than the NUV at a slight cost to PAE. Finally, comparing the FG UV and CFG UV trajectories, the former produces a 0.7 dB improvement in NPR with only 0.6 pp reduction in PAE.

Conclusion

The design and measurement of an octave bandwidth 10 W supply modulated GaN MMIC PA is presented. The PA is deliberately designed for peak PAE at 15 V, in a nominally 20-V process, to have a higher average PAE when dynamically supply modulated. Across the entire bandwidth, the PAE is greater than 23.0% over 10 dB of back-off power by utilizing a voltage range of 6 to 20 V. This approach is validated by measurements at 6.5 GHz using a four-level discrete supply modulator and a 10 MHz multi-carrier noise-like signal with a PAPR of 10.6 dB. Through use of a flat-gain trajectory with uniform voltage spacing, the NPR is improved by 2.5 dB over the 20 V static case at an average output power of 35 dBm with 3.8 percentage points improved PAE. For a desired NPR of 20 dB the PAE is improved by 5.5 and 9.8 percentage points over the 10 and 20 V case, respectively.

Acknowledgement

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