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Terahertz Planar Goubau Line Components on Thin Suspended Silicon Substrate

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Abstract—The planar Goubau line is a low-loss planar single-conductor waveguide that holds promise for terahertz applications, where power efficiency is crucial. We present three circuit elements for planar Goubau line: a stopband filter, a matching load, and a power divider, which have been fabricated in a high-resistivity silicon membrane. Simulation results are presented for the matching load and the power divider. The filter’s performance is validated by comparing measurement results with simulations, showing good agreement.

THE planar Goubau line (PGL) [1], [2] is a planar waveguide consisting of a single metal strip deposited on a dielectric substrate. Its single conductor allows a quasi-transverse-magnetic mode whose field distribution decays exponentially in the axial direction, thus having a large extension [2]. This extensive field distribution can excite propagating modes in the substrate with a higher phase constant and thus increase losses. However, if a sufficiently electrically-thin substrate is used, the radiation losses of the PGL will be minimized [3]. This, together with its lower conductor losses, makes the PGL more power-efficient than other planar transmission lines at terahertz frequencies [4], where minimizing energy losses becomes crucial.

Some circuit elements have been proposed for PGL [5], [6] but further work is needed to develop a broader range of components to enable more complex RF systems for this power-efficient waveguide. A challenge for the design of PGL circuit elements lies in that, being a single conductor waveguide, many of the design strategies for two-conductor transmission lines do not hold.

We present three fundamental circuit elements for PGL designed for terahertz frequencies: a stopband filter, a matching load, and a power divider. These elements have been designed with 350-nm gold on a 10 μm thick high-resistivity silicon-membrane substrate ($\epsilon_r = 11.7 - j2 \cdot 10^{-4}$, in bulk) in a silicon-on-insulator chip, minimizing radiation loss, and providing better mechanical strength and repeatability than our previously presented plastic film substrate [4]. The silicon membrane was made by etching the buffer in the silicon-on-insulator chip. The three devices were designed using 3D electromagnetic simulations using finite integration technique (CST Studio Suite) from 0.75 THz to 1.1 THz. The S-parameters of the fabricated filter were measured using a vector network analyzer (Keysight PNA-X with VDI WR1.0 frequency extenders) and ground-signal-ground contact probes (DMPI T-wave GSG probes, with 25 μm probe pitch). Measurements were calibrated using a previously developed multi-

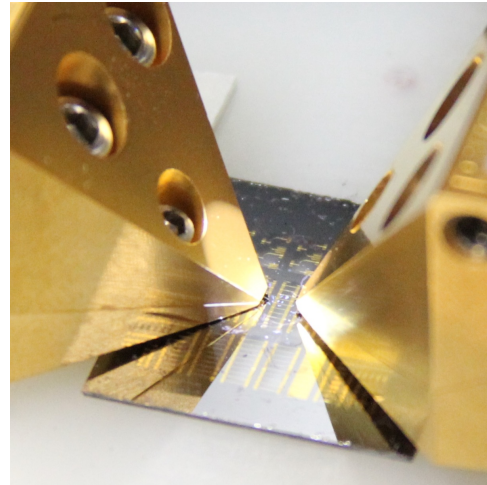


Fig. 1. Photograph of the ground-signal-ground probes measuring the S-parameters of the proposed filter on a silicon membrane, contained in the square silicon-on-insulator chip.

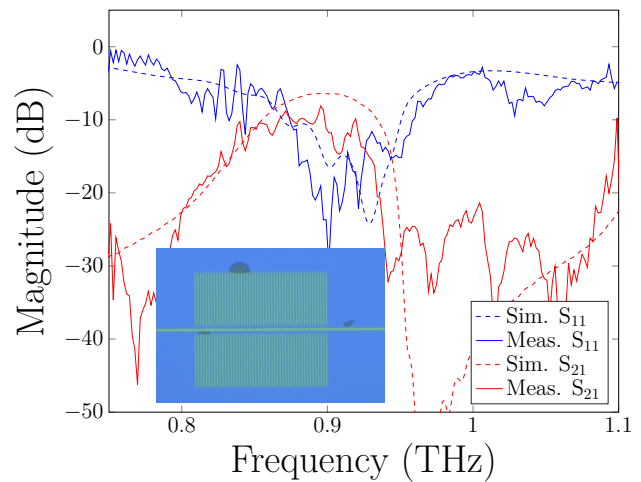


Fig. 2. **Stopband filter.** Comparison of measured and simulated S-parameter results of the filter, showing pass- and stopbands. Inset shows a micrograph of the fabricated filter.

line TRL calibration for PGL [7], included in the same wafer as the devices under test. The chip containing the devices on the membrane was measured on top of a polyethylene supporting substrate (Fig. 1) to avoid coupling with the metal chuck of the probe station.

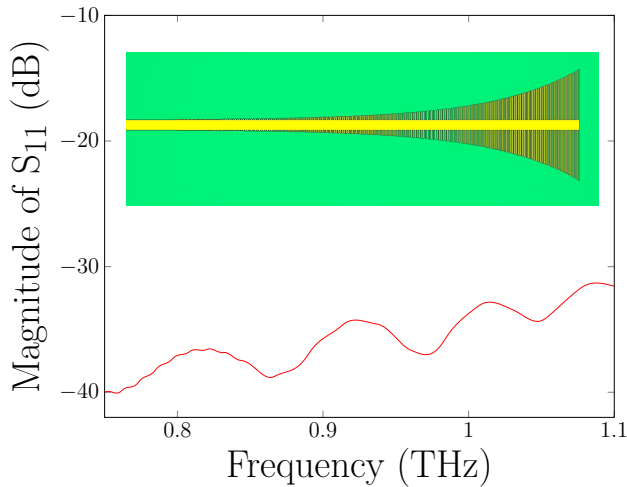


Fig. 3. **Matched load.** Simulated results of the magnitude of S_{11} versus frequency, showing excellent return loss. Inset shows the layout, where yellow represents gold and green the high-resistivity silicon membrane.

The stopband filter consists of periodical half-wavelength resonators laid perpendicular to the PGL (inset in Fig. 2), which produce pass- and stopbands. It has the advantage of being easily tuned by adjusting the lengths of the resonating lines. A detailed description of the working principle of the filter can be found in [8].

The proposed PGL matched load (Fig. 3) consists of a progressively corrugated PGL. This load has shown simulated results of return loss higher than 31 dB across the bandwidth. This exceptional performance could open the possibility of using such matched load for calibration standards [7] and measuring the S-parameters of multi-port devices with terminated ports.

Finally, the proposed power divider (Fig. 4) is based on a PGL short-circuit [7], which couples the power into two perpendicular PGL lines. Simulation results show an input port (port 1) matching better than -11 dB and -9dB in the output ports (ports 2 and 3), an insertion loss of around 6 dB, and isolation between output ports of at least 10 dB. This power divider couples more power to the output ports and has a better input port match than a regular tee-shaped power divider, which had high radiation loss for PGL.

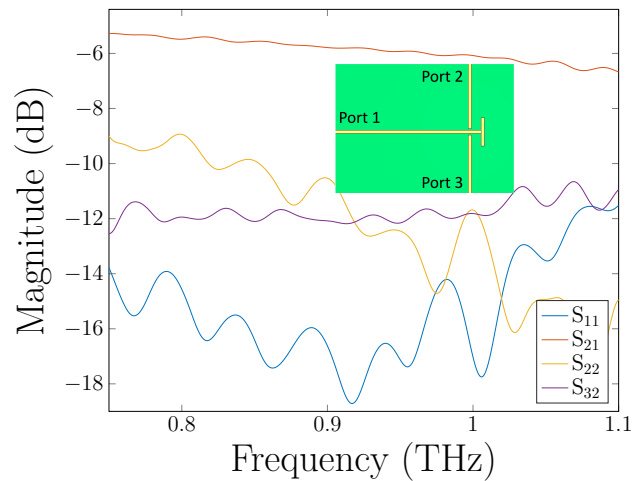


Fig. 4. **Power divider.** Simulated S-parameters versus frequency of the proposed power divider. Inset shows the layout, where yellow represents gold and green the high-resistivity silicon membrane.

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