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Capacitor Voltage Balancing of a Grid-Tied, Cascaded Multilevel Converter with Binary Asymmetric Voltage Levels Using an Optimal One-Step-Ahead Switching-State Combination Approach †

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Abstract: This paper presents a novel capacitor voltage balancing control approach for cascaded multilevel inverters with an arbitrary number of series-connected H-Bridge modules (floating capacitor modules) with asymmetric voltages, tiered by a factor of two (binary asymmetric). Using a nearest-level reference waveform, the balancing approach uses a one-step-ahead approach to find the optimal switching-state combination among all redundant switching-state combinations to balance the capacitor voltages as quickly as possible. Moreover, using a Lyapunov function candidate and considering LaSalle's invariance principle, it is shown that an offline calculated trajectory of optimal switching-state combinations for each discrete output voltage level can be used to operate (asymptotically stable) the inverter without measuring any of the capacitor voltages, achieving a novel sensorless control as well. To verify the stability of the one-step-ahead balancing approach and its sensorless variant, a demonstrator inverter with 33 levels is operated in grid-tied mode. For the chosen 33-level converter, the NPC main-stage and the individual H-bridge modules are operated with an individual switching frequency of about 1 kHz and 2 kHz, respectively. The sensorless approach slightly reduced the dynamic system response and, furthermore, the current *THD* for the chosen operating point was increased from 3.28 % to 4.58 % in comparison with that of using the capacitor voltage feedback.

Keywords: modular multilevel converters; multilevel systems; power supplies; sensorless control; total harmonic distortion

1. Introduction

Multilevel converters (MLC) are commonly used for high voltage applications in power systems [1,2] or, sometimes, these are even suggested for large electric drives [3,4]. Lately, multilevel inverters are gaining in interest for low voltage applications ($V < 1\,\mathrm{kV}$) due to their advantages in comparison to two-level converters, such as fault-tolerant operation capability [5,6], reduced common mode noise emissions [7,8] and the application of cheap, energy efficient low-voltage MOSFETs [9–11].

In [12–14], the topology of a cascaded H-bridge or a hybrid MLC (NPC mainstage) is shown. The additional series-connected H-bridges should help to lower the amount of output voltage harmonics and, thus, to reduce the size of the passive components, such as the grid or EMI-filter, or to improve the output current quality. To properly operate an MLC with capacitor modules, the capacitor voltages must be balanced. Therefore, several balancing algorithms can be found for symmetric MLCs [15–19]. As for example described in [15], self-balancing is typically achieved when using phase-shifted PWM, which introduces additional differential mode harmonics, lowering the current THD. Using asymmetric DC link voltage levels for the series-connected H-bridges can increase the output waveform's quality, whereas the possibility to balance the capacitor voltages is compromised [14,20,21]. As stated in [14,21], the charge balance control for an asymmetric inverter with a voltage ratio of three cannot be achieved. To overcome this problem, only isolated voltage sources, charged from the mains, such as described in [22], or supplied by additional DC converters, as shown in [23], could be used. This approach requires a rectifier stage or a DC converter for each H-bridge module, introducing additional system costs. The authors of [24] suggest to replace only a limited selection of capacitor modules by additional isolated voltage sources, acting as charge buffers. Similarly, in [14,25,26] it is suggested to combine a number of redundant high and low resolution cells, which help to maintain the capacitor charge balance, whereas the number of output levels is reduced.

In contrast, to maintain a high number of output levels and to properly balance the individual capacitor voltages, an asymmetric voltage grading by a factor of two (binary asymmetric) is suggested as a compromise in [12,27–30]. As described in [12,28], a predetermined switching scheme relative to the modulation index and the displacement power factor can be used to maintain the capacitor charge balance when using a voltage grading ratio of two. However, in [28] only one capacitor module is considered and a predetermined switching scheme, as in [12], requires a large memory for the lookup table. In [31–33] it is shown that a predetermined switching pattern can be even used to operate the inverter without measuring the capacitor voltages. Nonetheless, in [31–33] only a symmetric MLC is considered. In contrast, the authors of [29] suggest a self-balancing modulation scheme for binary asymmetric MLCs without measuring (sensorless) the floating capacitors' voltages. The suggested modulation scheme in [29] alternatively utilizes redundant switching-sate combinations, referred to as cell-voltage combinations. When using the approach in [29] with nearest-level control, the capacitors' charges are balanced over several electrical fundamental periods and, thus, according to [30], big capacitors are required. Therefore, in [29] the binary asymmetric inverter is operated with PWM and, thus, the provided solution actually resembles a generic self-balancing approach, typically achieved phase-shifted PWM [15].

Research Contribution and Scope

As an extended post-conference article of [34], the research contribution of this paper is two-fold. First, a novel balancing algorithm for the capacitor voltages of a binary asymmetric cascaded multilevel inverter is derived. The suggested algorithm uses an optimal, one-step-ahead switching-state combination approach to balance the capacitor voltages as quickly as possible. In comparison to that of the methods available in [14–18,24,28–30], the presented algorithm utilizes a low switching frequency (couple of kHz) and it achieves a quick dynamic response without requiring any additional hardware. Moreover, it can be easily applied to higher level asymmetric MLCs operated with nearest-level control (NLC). Second, with the help of a Lyapunov function, based on the energy stored in the grid filter and the capacitor modules, and considering LaSalle's invariance principle, it is shown that an offline calculated trajectory of optimal switching-state combinations for each discrete output voltage level can be used to operate (asymptotically stable) the inverter without measuring any of the capacitor voltages, achieving a novel self-balancing approach as well. In comparison to that of the sensorless approach in [29], the capacitance requirement according to [30] for NLC is reduced and only a small lookup table is required.

To experimentally verify the effectiveness of the optimal, one-step-head switching-state combination approach and its sensorless variant, a demonstrator inverter from Imperix Ltd. and a simple, inductive grid filter is used. The setup is operated in grid-tied operation feeding active power to the grid. Within the scope of this paper, the converter and the grid filter design is not considered, since the major focus lies on the voltage balancing algorithm.

2. Asymmetric Cascaded Multilevel Converter Basics

The topology of a grid-connected, asymmetric, hybrid multilevel converter based on an NPC main stage and n cascaded H-bridges, can be seen in Figure 1. Due to the voltage grading of adjacent converter modules, this topology is referred to as exponential modular multilevel converter (EMMC) in [27]. Using an NPC mainstage configuration, the depicted single-phase EMMC can be easily extended to a three-phase converter. The 800 V NPC mainstage could be replaced by a 400 V H-bridge stage. Then, the converter would resemble a generic cascaded H-bridge converter with asymmetric capacitor voltages. Therefore, the presented theory can be easily applied to different variants of cascaded or hybrid multilevel inverters.

For simplicity, a lossy L-filter with an inductance L_{filter} and a series resistance R_{filter} is chosen as a grid-filter within the scope of this paper's analysis. Alternatively to a pure inductive filter, an LCL-filter could be chosen, as for example described in [35,36]. The DC link voltage V_{DC} must be larger than the peak value of the grid voltage ($V_{\text{AC,pk}} = \sqrt{2} \times 230\,\text{V}$) to control both the active and the reactive power flow. For example, for a sufficient control margin, it might be suitable to chose a DC link voltage of $V_{\text{DC}} = 350\,\text{V}$. To charge up the capacitors to the their desired reference voltages, a charging resistor R_{charging} is initially used. During normal operation, the charging resistor R_{charging} is bypassed.

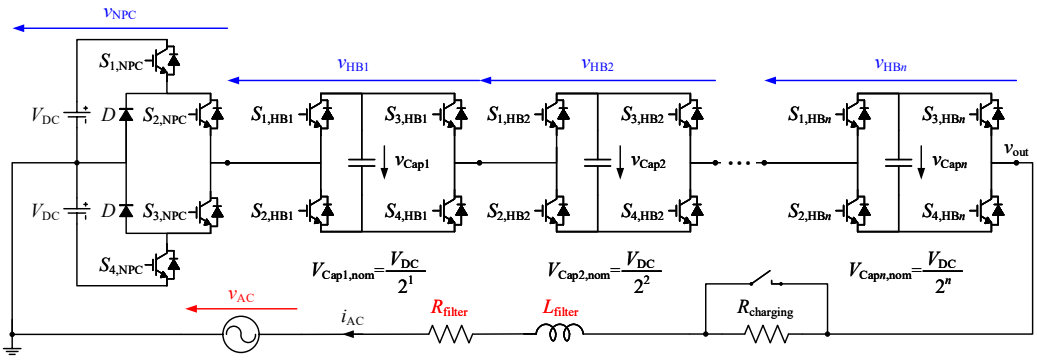


Figure 1. Grid-connected, single-phase asymmetric MLC arrangement, using an NPC module as main stage and n series-connected H-bridges, with charging resistor R_{charging}.

2.1. Switching-States

The semiconductor switches of the main stage (NPC module) are operated in pairs and only adjacent switches should be activated at the same time. If three switches in series are activated, as for example $S_{1,\text{NPC}}$, $S_{2,\text{NPC}}$ and $S_{3,\text{NPC}}$, one DC source is short-circuited. Therefore, the switching-state of the NPC main stage relative to the individual switches' states can be expressed as

$$S_{\text{NPC}} = \{1, 0, -1\} = S_{1,\text{NPC}} S_{2,\text{NPC}} - S_{3,\text{NPC}} S_{4,\text{NPC}} \tag{1}$$

and, thus, the output voltage of the NPC stage becomes

$$v_{\text{NPC}} = V_{\text{DC}} S_{\text{NPC}} \quad . \tag{2}$$

The nominal reference voltages of the series-connected H-bridges are tiered by a factor of two. Similar to the NPC module, the switches of each H-bridge are operated in pairs. If the two upper (S_{1,HB_i} and S_{3,HB_i}) or the two lower switches (S_{2,HB_i} and S_{4,HB_i})

are activated, the voltage source (capacitor module) is bypassed. If the switches are operated diagonally, the corresponding voltage source (capacitor module) is inserted in forward (S_{2,HB_i} and S_{3,HB_i}) and reverse (S_{1,HB_i} and S_{4,HB_i}) direction into the phase strand, respectively. Consequently, the switching-state of each H-bridge relative to the individual switches' states, can be expressed as

$$S_{\mathrm{HB}_i} = \{1, 0, -1\} = S_{2,\mathrm{HB}_i} S_{3,\mathrm{HB}_i} - S_{1,\mathrm{HB}_i} S_{4,\mathrm{HB}_i} \tag{3}$$

which can be used to express the output voltage of each H-bridge according to

$$v_{\mathrm{HB_i}} = \frac{V_{\mathrm{DC}}}{2^i} S_{\mathrm{HB_i}} \tag{4}$$

with $i = 1, 2, \cdots, n$. Using (2) and (4) the output voltage of the asymmetric MLC can be expressed as

$$v_{\mathrm{out}} = V_{\mathrm{DC}} S_{\mathrm{NPC}} + \sum_{i=2}^{n} S_{\mathrm{HB}i} \frac{V_{\mathrm{DC}}}{2^i} \tag{5}$$

while the switching-state vector can be defined as

$$S_{\mathrm{MLC}} = \begin{bmatrix} S_{\mathrm{NPC}} \\ S_{\mathrm{HB1}} \\ \vdots \\ S_{\mathrm{HB_n}} \end{bmatrix}' \quad . \tag{6}$$

With n H-bridge modules, the number of output voltage levels L can be expressed as

$$L = 2^{n+1} + 1 \quad . \tag{7}$$

2.2. Nearest-Level Control

A simple approach to modulate the desired sinusoidal output voltage waveform is nearest-level control (NLC), as described in [13]. The fundamental component can be approximated with the help of the modulation index M according to

$$\hat{V}_{\mathrm{out},1} \approx V_{\mathrm{DC}} M \quad \text{with} \quad V'_{\mathrm{DC}} = \frac{2V_{\mathrm{DC}}}{L-1} \quad . \tag{8}$$

With the help of the pulse transition angle vector

$$\alpha = \begin{bmatrix} \alpha_1 \; \alpha_2 \; \ldots \; \alpha_{\frac{L-1}{2}} \end{bmatrix}^{\mathrm{T}} \tag{9}$$

the staircase-shaped output voltage waveform can be expressed as

$$v'_{\mathrm{out,ref}}(\omega t) = \sum_{j=1}^{\frac{L-1}{2}} V'_{\mathrm{DC}} \Gamma_j(\omega t) \tag{10}$$

with

$$\Gamma_j(\omega t) = \begin{cases} +1; & \text{if } \alpha_j \leq \omega t \leq \pi - \alpha_j \\ -1; & \text{if } \pi + \alpha_j \leq \omega t \leq 2\pi - \alpha_j \\ 0; & \text{else} \end{cases} \quad . \tag{11}$$

If the modulation index is low, not all voltage levels are needed. With respect to α, the number of needed pulse transition angles can be calculated according to

$$k = \left\lceil \frac{M(L-1)}{2} \right\rceil \tag{12}$$

where the operator $\lceil\ \rceil$ indicates to round up the result of the fraction to the nearest integer value. The value of the pulse transition angles can be calculated according to

$$(j-0.5)V'_{\mathrm{DC}} = \frac{(2j-1)V_{\mathrm{DC}}}{L-1} = V_{\mathrm{DC}} M \sin(\alpha_n) \tag{13}$$

which results in

$$\alpha_j = \arcsin\left(\frac{2j-1}{(L-1)M}\right) \quad . \tag{14}$$

Consequently, the pulse transition angle vector α becomes

$$\alpha = \begin{bmatrix} \alpha_1 = \arcsin\left(\frac{1}{(L-1)M}\right) \\ \vdots \\ \alpha_k = \arcsin\left(\frac{2k-1}{(L-1)M}\right) \\ \alpha_{k+1} = \frac{\pi}{2} \\ \vdots \\ \alpha_{\frac{L-1}{2}} = \frac{\pi}{2} \end{bmatrix} \quad . \tag{15}$$

For example, Figure 2 depicts the modulated staircase-shaped output voltage (phase voltage) waveform using NLC for a 17-level converter ($n = 3$ according to Figure 1) and a modulation index $M = 0.95$.

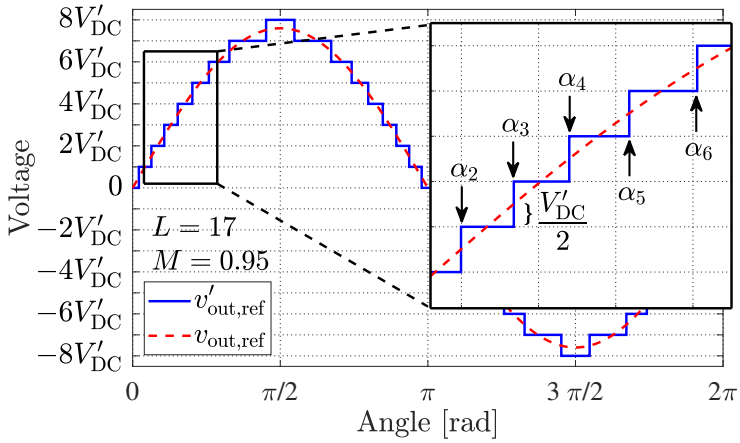


Figure 2. Desired, modulated reference voltage waveform $v'_{\mathrm{out,ref}}$ using nearest-level control for a 17-level converter and a modulation index $M = 0.95$.

Under nominal operating conditions, a single-phase, grid-connected inverter with a DC link voltage of 350 V is typically operated with a modulation index in the range of 0.85 to 0.95. Nonetheless, according to the IEEE Std. 2030 [37], "IEEE Guide for Smart Grid Interoperability of Energy Technology and Information Technology Operation with the Electric Power System (EPS),, End-Use Applications, and Loads", grid-feeding converters shall be able to continue their operation during certain fault conditions, such as a low-voltage ride-through condition. Therefore, grid-connected converters, when operated in grid-feeding mode, must be able to operate with low modulation indices in the range from 0.15 to 0.25 [38]. Therefore, it is reasonable to employ a large number (>30) of output voltage levels for MLIs operated with NLC.

3. Weighted Total Harmonic Distortion of Higher Level NLC Waveform in Comparison to Three-Level PWM

This section should briefly quantify the quality of higher level NLC waveforms in relation to a three-level PWM waveform and its switching frequency.

The concept of the Weighted Total Harmonic Distortion (*WTHD*), as explained in [13], is a measure to compare the probable current quality of different voltage waveforms. To derive the expression of the *WTHD*, it is reasonable to start from the voltage *THD* expression, which can be described as

$$THD_{\mathrm{V}} = \sqrt{\left(\frac{V_{\mathrm{rms}}}{V_{1,\mathrm{rms}}}\right)^2 - 1} \quad . \tag{16}$$

Without a DC component, the voltage *THD* expression becomes

$$THD_{\mathrm{V}} = \sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{V_1}\right)^2} \quad . \tag{17}$$

Similar as in (17), the current *THD* can be expressed as

$$THD_{\mathrm{I}} = \sqrt{\sum_{h=2}^{\infty}\left(\frac{I_h}{I_1}\right)^2} \quad . \tag{18}$$

Assuming that the voltage is applied to a lossless inductive load, the current harmonics can be calculated with the help of the voltage harmonics according to

$$I_h \approx \frac{V_h}{h\omega_1 L} \quad \text{with} \quad h = \{2,3,4\cdots\} \quad . \tag{19}$$

Inserting (19) in the current *THD* expression given in (19), the weighted *THD* as a function of the voltage harmonics can be obtained according to

$$WTHD = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2} \quad . \tag{20}$$

According to [13], using NLC, the output harmonic components relative to the pulse transition angles can be expressed as

$$V_{\mathrm{out},h} = \frac{8V_{\mathrm{DC}}}{(L-1)h\pi}\left(\cos(h\alpha_1) + \cdots + \cos(h\alpha_{\frac{L-1}{2}})\right) \tag{21}$$

with only odd harmonic components occurring, corresponding to $h = \{1,3,5,\cdots\}$. In comparison, when operating only the NPC main stage, the output voltage components using three-level, naturally sampled, sine-triangle PWM can be described according to [13] as

$$V_{\mathrm{out},1} = V_{\mathrm{DC}}M \tag{22}$$

and

$$V_{\mathrm{out},h} = \frac{4V_{\mathrm{DC}}}{\pi}\sum_{c=1}^{\infty}\sum_{b=-\lambda}^{\lambda}\frac{1}{2c}J_{2b-1}(c\pi M)\cos([c+b-1]\pi) \tag{23}$$

with

$$h = 2cm_{\mathrm{f}} + (2b-1) \quad . \tag{24}$$

The expression $J_{2\mathrm{b}-1}(c\pi M)$ denotes the Bessel functions of the first kind with c representing the order of the carrier harmonic and b representing the order of the corresponding sideband

harmonic. The number/boundary of the considered sideband harmonics is λ, which is dependent on the carrier ratio

$$m_f = \frac{f_{sw}}{f_1} \quad , \tag{25}$$

which is usually considered to be an integer value. In practice, also to avoid overlapping, λ is typically selected to be less than 10, because of the rapid roll-off in magnitude of the Bessel function $J_{2b-1}(c\pi M)$ [13].

With the help of (21) and (23) the weighted *THD WTHD*, as described in (20), can be determined for NLC and three-level PWM relative to the modulation index M, as depicted in Figure 3. A grid-tied, 33-level inverter operated with NLC theoretically achieves a similar current quality as a three-level inverter operated with a switching frequency f_{sw} of 5 kHz to 25 kHz.

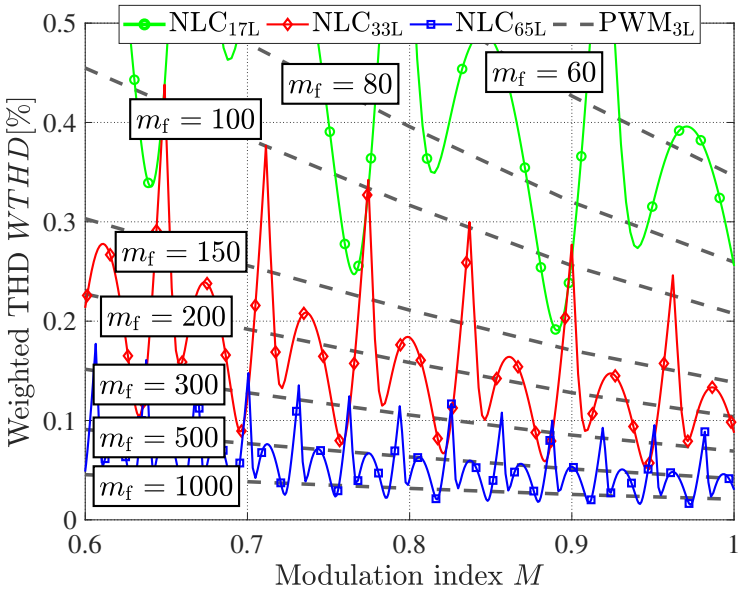


Figure 3. Weighted *THD WTHD* relative to the modulation index M when using NLC, computed for 17, 33, and 65 output voltage levels, and three-level PWM for different carrier frequency ratios m_f.

4. Current Control and Voltage Balancing of the Asymmetric Cascaded Multilevel Converter

This section gives a brief description of the current control of a grid-tied, asymmetric cascaded MLC, as shown in Figure 1. Furthermore, as a main contribution of this paper, the novel capacitor voltage balancing approach and its sensorless variant are derived.

Typically, the apparent power at the grid side, can be determined as

$$P_{AC} + jQ_{AC} = V_{AC} \cdot I_{AC}^{*} \quad . \tag{26}$$

Thus, the desired reference current for a certain apparent power can be calculated as

$$I_{AC,ref} = \frac{P_{AC,ref} - jQ_{AC,ref}}{V_{AC}^{*}} \quad . \tag{27}$$

A phase-locked loop (PLL) based on a second order generator, as described in [39], shall be used to to synchronize the voltage reference frame of the inverter with the grid voltage V_{AC}.

4.1. Current Control Using a Proportional-Resonant Controller

The suggested control scheme of the output current i_{AC} for the grid-tied, asymmetric cascaded MLC (shown in Figure 1) is depicted in Figure 4 and explained in the following.

The derivative of the output current i_{AC} can be expressed as

$$\frac{di_{AC}}{dt} = -\frac{R_{filter}}{L_{filter}} i_{AC} + \frac{1}{L_{filter}} (v_{out} - v_{AC}) \tag{28}$$

with v_{out} as described in (5). Using the Laplace transform of (28), the current i_{AC} in relation to the output voltage v_{out} can be expressed in transfer-function form as

$$G_p(s) = \frac{i_{AC}}{v_{out} - v_{AC}} = \frac{1}{sL_{filter} + R_{filter}} \quad . \tag{29}$$

To control a sinusoidal single-phase current through the grid filter, a Proportional-Resonant (PR) controller, as described in [40] and emphasized in green in Figure 4, can be used. Its gain can be mathematically expressed as

$$G_c(s) = \frac{v_{out,ref} - v_{AC}}{\Delta i_{AC}} = K_p + \frac{K_i s}{s^2 + \omega_0^2} \tag{30}$$

which corresponds to

$$G_c(s) = K_p + \frac{K_i \frac{1}{s}}{1 + \omega_0^2 \frac{1}{s} \frac{1}{s}} \quad . \tag{31}$$

As described in [41], to discretize the controller in (31), both the forward Euler method according to

$$\frac{1}{s} \rightarrow T_s \frac{1}{z-1} \tag{32}$$

as well as the backward Euler method according to

$$\frac{1}{s} \rightarrow T_s \frac{z}{z-1} \tag{33}$$

can be used to implement the integrator terms and preserve the properties of the continuous PR-controller. Thus, as suggested in [41], a combination of both methods is used: forward Euler for the integrator term in the numerator and the first integrator in the denominator, and backward for the second integrator term in the denominator. The resulting controller gain $G_c(s)$ transformed into the z-domain is

$$G_c(z) = K_p + K_i T_s \frac{z-1}{z^2 - z(2 - \omega_0^2 T_s^2) + 1} \quad . \tag{34}$$

When using PWM, the sample time T_s is typically the inverse of the switching frequency f_{sw} at which the entire converter leg is operated. The controller parameters K_i and K_p can be parametrized in a similar manner as for a PI-controller, for example as described in [42,43]. To improve the performance of the current controller, the measured grid voltage v_{AC} was used in here as a feedforward term, as can be seen in Figure 4. Hence, the current controller determines the required output voltage $v_{out,ref}$, which should be modulated by the nearest discrete output voltage level $v'_{out,ref}$. Then, an optimal switching-state combination should be chosen and applied to actually output the required voltage.

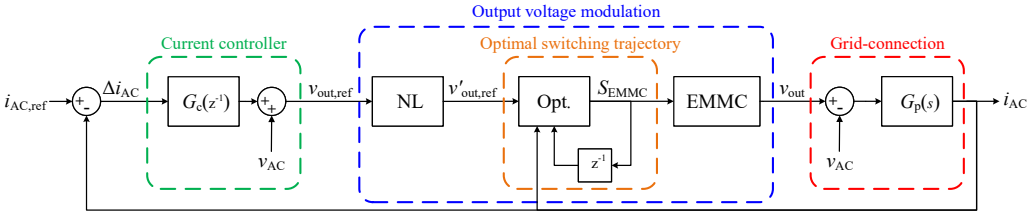


Figure 4. Current control scheme of asymmetric MLC.

4.2. Capacitor Voltage Balancing Using a One-Time-Step Model Predictive Control Approach

To properly control the current, the capacitor voltages must be balanced according to their nominal rating by the alternate selection of optimal switching-state combinations, as highlighted in orange in Figure 4. In the following, a model predictive control (MPC) approach with a prediction horizon of one time step, which is often referred to as one-step ahead approach [44,45], is introduced to find the optimal switching-state vector to mitigate the capacitors' voltage imbalance within the next switching interval as much as possible.

The dynamics of the capacitors' voltages, according to Figure 1, can be described as

$$\frac{dv_{\mathrm{Cap_i}}}{dt} = -\frac{1}{C_i} S_{\mathrm{HB_i}} i_{\mathrm{AC}} \tag{35}$$

with $i = 1, 2, \cdots, n$. The deviation of the capacitors' voltages relative to their nominal reference voltages can be expressed as

$$\Delta v_{\mathrm{Cap}} = \begin{bmatrix} v_{\mathrm{Cap1}} \\ v_{\mathrm{Cap2}} \\ \vdots \\ v_{\mathrm{Cap}n} \end{bmatrix} - \begin{bmatrix} V_{\mathrm{Cap1,ref}} \\ V_{\mathrm{Cap2,ref}} \\ \vdots \\ V_{\mathrm{Cap}n\mathrm{,ref}} \end{bmatrix} . \tag{36}$$

For each output voltage level of the EMMC, there are m switching-state combinations according to

$$S_{\mathrm{MLC}_m} = \begin{bmatrix} S_{\mathrm{NPC},1} & S_{\mathrm{HB1},1} & \cdots & S_{\mathrm{HB}n,1} \\ \vdots & \vdots & \ddots & \vdots \\ S_{\mathrm{NPC},m} & S_{\mathrm{HB1},m} & \cdots & S_{\mathrm{HB}n,m} \end{bmatrix} . \tag{37}$$

Thus, considering just the switching-states of the H-bridges comprising the capacitor modules, S_{MLC_m} can be reduced to

$$S_{\mathrm{HB}_m} = \begin{bmatrix} S_{\mathrm{HB1},1} & \cdots & S_{\mathrm{HB}n,1} \\ \vdots & \ddots & \vdots \\ S_{\mathrm{HB1},m} & \cdots & S_{\mathrm{HB}n,m} \end{bmatrix} . \tag{38}$$

Consequently, the weighting vector W, relative to the direction of the current, to assess the effectiveness of each individual switching-state combination can be calculated as

$$W = \begin{cases} +S_{\mathrm{HB}_m} \cdot \Delta v_{\mathrm{Cap}} & \text{for } i_{\mathrm{AC}} \geq 0 \\ -S_{\mathrm{HB}_m} \cdot \Delta v_{\mathrm{Cap}} & \text{for } i_{\mathrm{AC}} < 0 \end{cases} . \tag{39}$$

Thus, the switching combination achieving the maximum value of W yields the optimal switching-state combination according to

$$\max(W) \rightarrow S_{\mathrm{opt}} \quad . \tag{40}$$

To understand the suggested approach better, a short example is given in the following. The output voltage v_{out} should be $\frac{V_{\mathrm{DC}}}{2^4}$ and the current is positive according to $i_{\mathrm{AC}} \geq 0$.

The number of H-bridge modules is $n = 4$. This results in $m = 5$ possible switching-state combinations as stated in Table 1.

Table 1. Switching-state combinations for $v_{\text{out}} = \frac{V_{\text{DC}}}{2^4}$ and $n = 4$, which gives $m = 5$ possible combinations.

$S_{\text{NPC}}\left(\frac{V_{\text{DC}}}{2^0}\right)$	$S_{\text{HB1}}\left(\frac{V_{\text{DC}}}{2^1}\right)$	$S_{\text{HB2}}\left(\frac{V_{\text{DC}}}{2^2}\right)$	$S_{\text{HB3}}\left(\frac{V_{\text{DC}}}{2^3}\right)$	$S_{\text{HB4}}\left(\frac{V_{\text{DC}}}{2^4}\right)$
1	−1	−1	−1	−1
0	1	−1	−1	−1
0	0	1	−1	−1
0	0	0	1	−1
0	0	0	0	1

Presumably, the first two capacitor modules are balanced, whereas the third and fourth show a deviation of −1 V and 2 V, respectively. Thus, the weighting vector can be calculated as

$$W = \begin{bmatrix} -1 & -1 & -1 & -1 \\ 1 & -1 & -1 & -1 \\ 0 & 1 & -1 & -1 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0\,\text{V} \\ 0\,\text{V} \\ -1\,\text{V} \\ 2\,\text{V} \end{bmatrix} \tag{41}$$

which results in

$$W = \begin{bmatrix} -1\,\text{V} \\ -1\,\text{V} \\ 1\,\text{V} \\ -3\,\text{V} \\ 2\,\text{V} \end{bmatrix} . \tag{42}$$

Finally, the optimal switching-state combination becomes

$$S_{\text{opt}} = [0\,0\,0\,0\,1] \quad . \tag{43}$$

A simple approach to properly dimension the capacitor sizes is given in [30]. As described in [30], the maximum voltage deviation of the converter's output voltage occurs when all modules are inserted and it can be approximated according to

$$\Delta V_{\text{out,max}} = \hat{I}_{\text{AC}} T_{\text{s}} \sum_{i=1}^{n} \frac{1}{C_i} \tag{44}$$

with $\hat{I}_{\text{AC}}$ and C_i being the phase current's amplitude and capacitance of the individual H-bridge modules, respectively. Thus, in comparison to the NLC approach in [30], the in here suggested approach can reduce the capacitor requirement according to (44), because the algorithm updates the switching-state combination with respect to the sample time T_{s} and not only when step-wise changes in the output voltage occur. Since the switching-state combination is not necessarily changed after each sample period, the suggested algorithm can be categorized as an MPC approach with variable switching time instants [46].

4.3. Sensorless Capacitor Voltage Balancing Using a Dynamic Programming Approach

Considering the suggested approach in Section 4.2, a series of offline calculated, optimal switching-state combinations for each discrete output voltage level and a series of current values, positive and negative, could be used to operate the inverter with a lookup table approach without measuring the actual capacitor voltages. Thus, the offline calculated optimal switching-state combinations are sequentially applied (z^{-1}), as shown in orange in Figure 4. This approach is referred to as dynamic programming.

To keep the capacitor voltages balanced, the optimal switching-state sequences simply need to drive the average capacitor currents, sometimes referred to as current-second areas (charge), to zero. Thus, considering a variation of the converter's displacement power factor and current amplitude, a large, intricate array of switching-state sequences would be required in theory. Although, when considering the illustration of the cell-voltage combinations in [24] [Figure 4], it becomes obvious that both the current-second and the applied voltage-second areas at steady state for any discrete output voltage become zero, if the EMMC itself is operated with a unity displacement power factor. Therefore, to reduce the required computational effort and the memory for the lookup table, the output current should be controlled to be in phase with the converter's output voltage, as depicted in Figure 5 for grid-feeding mode, which slightly reduces the actual power factor $\cos(\varphi)$. Nonetheless, this approach could affect the voltage stability when operating in grid-forming mode [47]. Consequently, an optimal switching-state sequence for each discrete voltage level when loaded with a DC current, achieving that the applied voltage-second areas of the H-bridge modules become zero, can be generated offline . The selected DC current value should preferably be as close as possible to the instantaneous current when the corresponding discrete level would be actually activated for the considered operating point. Nonetheless, if a different DC current is arbitrarily but reasonably chosen, the current-second areas become zero as well and, thus, only the capacitor voltages' ripples are marginally affected. The suggested sensorless approach is only suitable for MLCs operated with only active power capability. Due to symmetry reasons, it is sufficient to calculate the optimal switching-state combinations for only half of the discrete output levels, e.g., for the ones creating a positive output voltage. The switching-state combinations for the negative output levels can be obtained through the multiplication of the switching-state combinations for the positive output levels and minus one. For further simplifications, in here it is suggested to use the average absolute value of the selected operating point's AC current for all considered output levels when offline creating the switching-state combinations.

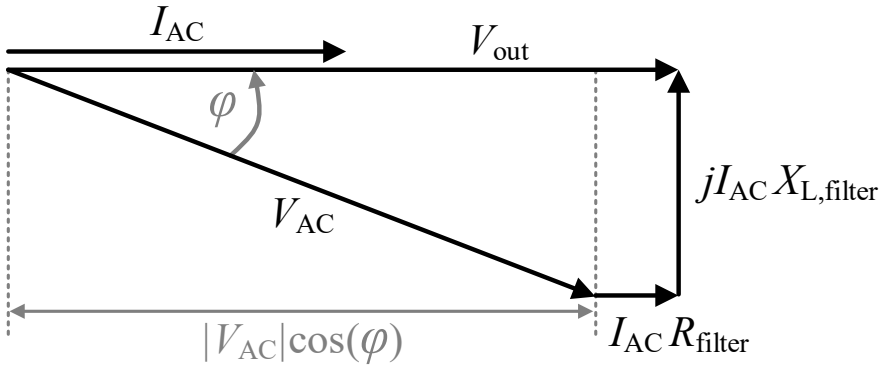
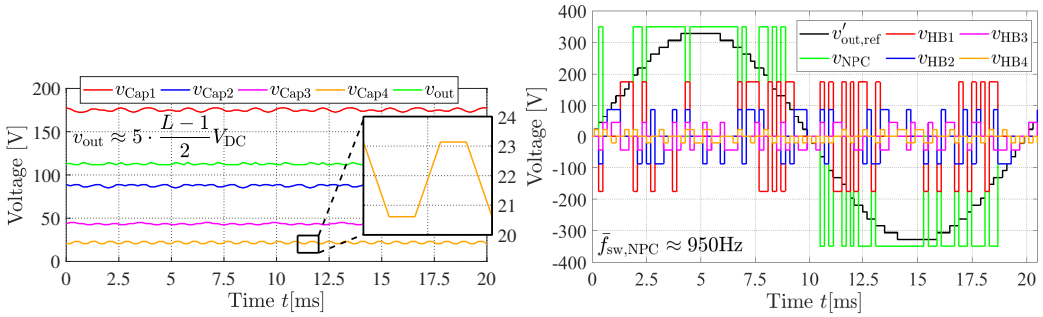


Figure 5. Vector diagram of controlled current I_{AC} relative to converter voltage V_{out} and grid voltage V_{AC} when operating converter in grid-feeding mode without capacitor voltage sensing.

For example, Figure 6a shows the simulated capacitor voltages and the output voltage, corresponding to the fifth positive output voltage level, for a 33-level EMMC while balancing the capacitors for a certain DC current considering the approach described in Section 4.2. Thus, the switching-state combinations obtained for Figure 6a should be stored in a lookup table, and the approach should be repeated for all remaining positive voltage levels. When operating the inverter and generating an AC output voltage, a switching-state combination is sequentially chosen from the stored lookup tables for each of the desired reference voltage levels $v'_{out,ref}$. For example, assuming ideally balanced capacitor voltages, Figure 6b shows the output voltages of the asymmetric MLC and the individual converter stages corresponding to a fundamental output voltage of $V_{out,1} = 330\,\mathrm{V}$.



a **b**

Figure 6. Switching-state sequence generation: (**a**) simulated capacitor voltage oscillations using the suggested one-time-step MPC approach for one discrete output voltage level and (**b**) generated switching-state sequence for one electrical period.

For the depicted switching pattern, the average switching frequency of the NPC main stage corresponds to about $\bar{f}_{\text{sw,NPC}} \approx 950\,\text{Hz}$, while the switching frequency of the individual H-bridges is about twice the switching frequency of the NPC module according to $\bar{f}_{\text{sw,HB}} \approx 2\bar{f}_{\text{sw,NPC}}$. Since the converter allows for bidirectional power flow, the described approach can be applied in a similar way when operating the converter as an electronic load.

5. Stability of the Sensorless, Dynamic Programming Approach

It is assumed that for some desired steady state current trajectory $i_{\text{AC,ref}}$ the required switching-state sequences $S_{\text{NPC}}^{(\text{des})}$ and $S_{\text{HB}\,i}^{(\text{des})}$, for achieving the necessary output voltage $v_{\text{out}} = V_{\text{DC}}\, S_{\text{NPC}}^{(\text{des})} + \sum_{i=1}^{n} S_{\text{HB}\,i}^{(\text{des})}\, v_{\text{Cap}\,i}$, can be accurately generated. This may eventually require a fine time resolution (or a relative high switching frequency). The developed converter system experimentally displays the following behavior: when driven by such an optimal switching-state sequence, independent of the initial state, the system eventually reaches the desired current trajectory. The goal of this section is proving such observed behavior.

The system considered is described by the current i_{AC} and n capacitor voltages $v_{\text{Cap}\,i}$, which represent together the state vector. The deviation between the actual state and the desired reference trajectory is described by

$$\Delta i_{\text{AC}} = i_{\text{AC}} - i_{\text{AC,ref}} \tag{45}$$

and

$$\Delta v_{\text{Cap}\,i} = v_{\text{Cap}\,i} - v_{\text{Cap}\,i,\text{ref}} \quad . \tag{46}$$

The dynamics of the actual and the reference current, both driven by the same optimal switching-state sequences $S_{\text{NPC}}^{(\text{des})}$ and $S_{\text{HB}\,i}^{(\text{des})}$, are given by

$$\frac{di_{\text{AC}}}{dt} = -\frac{R_{\text{filter}}}{L_{\text{filter}}} i_{\text{AC}} + \frac{1}{L_{\text{filter}}} (V_{\text{DC}} S_{\text{NPC}}^{(\text{des})} + \sum_{i=1}^{n} S_{\text{HB}\,i}^{(\text{des})} v_{\text{Cap}\,i} - v_{\text{AC}}) \tag{47}$$

and

$$\frac{di_{\text{AC,ref}}}{dt} = -\frac{R_{\text{filter}}}{L_{\text{filter}}} i_{\text{AC,ref}} + \frac{1}{L_{\text{filter}}} (V_{\text{DC}} S_{\text{NPC}}^{(\text{des})} + \sum_{i=1}^{n} S_{\text{HB}\,i}^{(\text{des})} v_{\text{Cap}\,i,\text{ref}} - v_{\text{AC}}) \tag{48}$$

respectively, such that the current error's dynamics become

$$\frac{d\Delta i_{\mathrm{AC}}}{dt} = -\frac{R_{\mathrm{filter}}}{L_{\mathrm{filter}}}\Delta i_{\mathrm{AC}} + \frac{1}{L_{\mathrm{filter}}}\sum_{i=1}^{n} S_{\mathrm{HB}\,i}^{(\mathrm{des})}\Delta v_{\mathrm{Cap}\,i} \quad . \tag{49}$$

Analogously, the dynamics of the actual and the reference capacitor voltages, both again driven by the same optimal switching-state sequences $S_{\mathrm{NPC}}^{(\mathrm{des})}$ and $S_{\mathrm{HB}\,i}^{(\mathrm{des})}$, are respectively given by

$$\frac{dv_{\mathrm{Cap}\,i}}{dt} = -\frac{1}{C_i}S_{\mathrm{HB}\,i}^{(\mathrm{des})} i_{\mathrm{AC}} \tag{50}$$

and

$$\frac{dv_{\mathrm{Cap}\,i,\mathrm{ref}}}{dt} = -\frac{1}{C_i}S_{\mathrm{HB}\,i}^{(\mathrm{des})} i_{\mathrm{AC,ref}} \tag{51}$$

leading to the following dynamics for the capacitors' voltage errors

$$\frac{d\Delta v_{\mathrm{Cap}\,i}}{dt} = -\frac{1}{C_i}S_{\mathrm{HB}\,i}^{(\mathrm{des})}\Delta i_{\mathrm{AC}} \quad . \tag{52}$$

The proof of the observed experimental behavior mentioned at the beginning of this section is easily shown by introducing the following Lyapunov function $V = V(\Delta i_{\mathrm{AC}}, \Delta v_{\mathrm{Cap}\,i})$ according to

$$V = \frac{L_{\mathrm{filter}}}{2}(\Delta i_{\mathrm{AC}})^2 + \sum_{i=1}^{n}\frac{C_i}{2}(\Delta v_{\mathrm{Cap}\,i})^2 \tag{53}$$

analogous in form to the total energy stored in the inductor and capacitors of the system, although now referred to the deviations from the desired trajectory. This Lyapunov function V is strictly positive as long as the errors Δi_{AC} and/or $\Delta v_{\mathrm{Cap}\,i}$ do not vanish. As a result of the dynamics (49) and (52) function V is a nonincreasing function with time

$$\frac{dV}{dt} = -R_{\mathrm{filter}}\Delta i_{\mathrm{AC}}^2 \quad . \tag{54}$$

This time derivative is nevertheless only negative semidefinite, since the Lyapunov function $V = V(\Delta i_{\mathrm{AC}}, \Delta v_{\mathrm{Cap}\,i})$ depends on all the $n+1$ dynamic variables, but its time derivative does only depend on one single variable (Δi_{AC}). Consequently, the original Lyapunov theorem is of no use for proving the asymptotic stability behavior Δi_{AC}, $\Delta v_{\mathrm{Cap}\,i} \overset{t\to\infty}{\longrightarrow} 0$ and the more general Krassowski–LaSalle invariance principle [48,49] is required. According to this latter principle, the dynamics asymptotically converge to some trajectory of the considered equations of motion (49) and (52), which simultaneously satisfied $dV/dt = 0$; however, a constant stationary point of the equations of motion is also a (trivial) trajectory remaining on the same value during the whole time evolution. A vanishing time derivative of the Lyapunov function yields

$$\frac{dV}{dt} = -R_{\mathrm{filter}}\Delta i_{\mathrm{AC}}^2 = 0 \quad \Rightarrow \quad \Delta i_{\mathrm{AC}} = 0 \quad , \tag{55}$$

which according to (49) leads to $\sum_{i=1}^{n} S_{\mathrm{HB}\,i}^{(\mathrm{des})}\,\Delta v_{\mathrm{Cap}\,i} = 0$, although not to the separated vanishing of each single $\Delta v_{\mathrm{Cap}i}$. Since nevertheless the switching-state sequence values $S_{\mathrm{HB}\,i}^{(\mathrm{des})}$ change all the time, once $\Delta i_{\mathrm{AC}} = 0$ is achieved, the probability of satisfying condition $\sum_{i=1}^{n} S_{\mathrm{HB}\,i}^{(\mathrm{des})}\,\Delta v_{\mathrm{Cap}\,i} = 0$ with varying $S_{\mathrm{HB}\,i}^{(\mathrm{des})}$ (and also changing $\Delta v_{\mathrm{Cap}\,i}$) is very low, particularly for a relative high number of capacitor modules: the only solution of condition $\sum_{i=1}^{n} S_{\mathrm{HB}\,i}^{(\mathrm{des})}\,\Delta v_{\mathrm{Cap}\,i} = 0$ under these conditions is therefore $\Delta v_{\mathrm{Cap}\,i} = 0$ for each single capacitor. Since this only solution $\Delta i_{\mathrm{AC}} = 0 = \Delta v_{\mathrm{Cap}\,i}$ is also a trajectory of the equations of motion, the Krassowski–LaSalle invariance principle shows that the system cannot get "stuck" at any other trajectory than such stationary point. Hence, when driving the con-

verter system with the optimal switching-state sequences corresponding to some desired reference trajectory, such trajectory is asymptotically reached

$$i_{\mathrm{AC}} \xrightarrow{t\to\infty} i_{\mathrm{AC,ref}} \quad \text{and} \quad v_{\mathrm{Cap}\,i} \xrightarrow{t\to\infty} v_{\mathrm{Cap}\,i,\mathrm{ref}} \quad . \tag{56}$$

The main ingredient in the previous proof is the existence of a nonvanishing (positive) resistance R_{filter} which constantly dissipates power, and thus, ensures the decreasing of the Lyapunov function value.

6. Measurements

To verify the effectiveness and the stability of the derived one-step ahead balancing algorithm and its sensorless variant (described above), a laboratory, 33-level converter is used, as can be seen in Figure 7. It is based on the commercially available converter modules from Imperix Ltd. and it comprises an NPC main stage [50] and four H-bridge modules [51]. The entire control and balancing algorithm is implemented in the B-Box RCP control unit [52] of Imperix Ltd. The DC inputs of the NPC module and each of the H-bridges are attached with a 517 µF and a 5 mF capacitor bank (electrolytic), respectively. The selected DC link voltage rating is $V_{\mathrm{DC}} = 350\,\mathrm{V}$, using unidirectional power supplies, and the chosen grid filter's inductance rating is about 30 mH ($L_{\mathrm{filter}} = 28.8\,\mathrm{mH}$, $R_{\mathrm{filter}} = 0.2\,\Omega$ and $I_{\mathrm{rat,rms}} = 30\,\mathrm{A}$). Here, the design of the converter and the grid filter is not part of this paper's scope. Especially, the size of the grid filter seems rather large, but it is chosen for simplicity. The inductance rating for an LCL-filter (60 dB damping per decade) with a similar damping effect could be about 100 times smaller, corresponding to about 300 µH. The used charging resistors have a total resistance of $R_{\mathrm{charging}} = 80\,\Omega$. The entire converter leg is operated with a sampling frequency of $f_{\mathrm{s}} = 5\,\mathrm{kHz}$, which results in an actual average switching frequency, similar as described in Section 4.3, of about $\bar{f}_{\mathrm{sw,NPC}} \approx 950\,\mathrm{Hz}$ and $\bar{f}_{\mathrm{sw,HB}} \approx 2\bar{f}_{\mathrm{sw,NPC}}$ for the NPC stage and the H-bridges, respectively. For the experimental verification, all waveforms are captured with an oscilloscope.

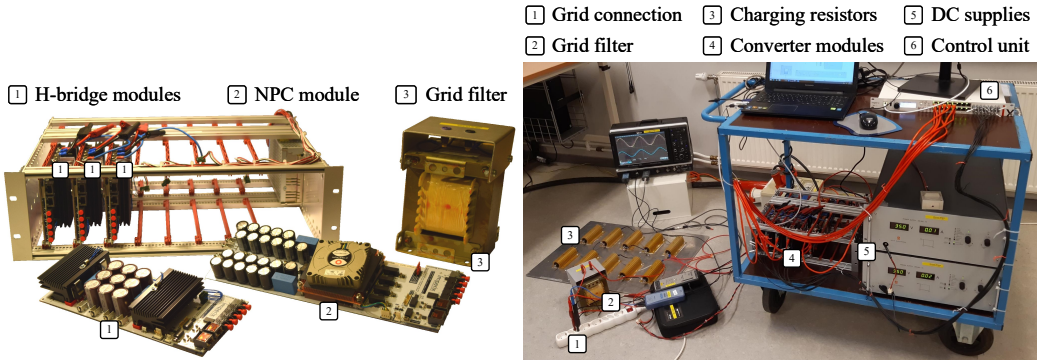


Figure 7. (**a**) Converter modules and grid filter. (**b**) Actual laboratory arrangement of the 33-level, grid-tied asymmetric MLC.

6.1. Capacitor Precharging

Before operating the converter in grid-feeding mode, the capacitors must be charged up using the suggested charging resistance R_{charging}. During the charging process, the reference output voltage $v_{\mathrm{out,ref}}$ should be set to v_{AC}. When already using the current controller, the reference current $i_{\mathrm{AC,ref}}$ should be set to zero. Figure 8a,b show the start-up charging of the H-bridges' capacitors when operating the inverter with and without the voltage sensing, respectively.

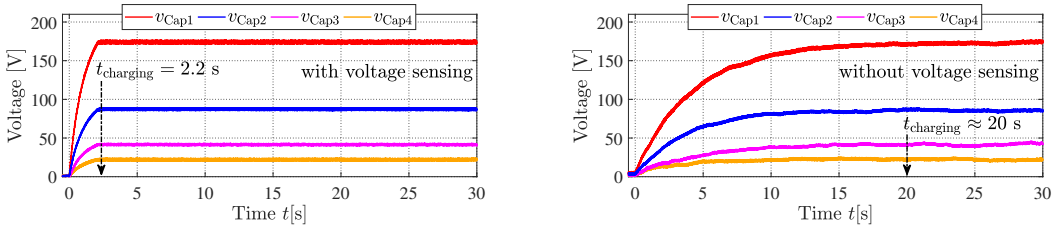


Figure 8. Measured charging of H-bridges' capacitors during converter startup using additional charging resistance $R_{\text{charging}} = 80\,\Omega$ (**a**), with sensing and (**b**) without sensing of the capacitor voltages.

Since the sensorless approach utilizes a switching-pattern, which was generated only for the actual operating point of $\hat{I}_{\text{AC}} = 10\,\text{A}$, it takes about 20 s until the capacitors have reached their nominal reference voltages. This in turn verifies the stability described in Section 5. On the contrary, when using the capacitor voltages as a feedback, the nominal reference voltages are already reached after about 2.2 s. Hence, the dynamic response, using the sensorless approach, is compromised.

6.2. Operation in Grid-Feeding Mode

When the H-bridges' capacitors are completely charged up, the charging resistor R_{charging} can be bypassed via the contactor. Subsequently, the converter can be operated according to Figure 5, feeding active power to the grid. Figure 9a,b show the grid voltage v_{AC}, the converter output voltage v_{out} and the output current i_{AC} for one electrical period with and without the sensing of the capacitor voltages, respectively. The current's magnitude is controlled to be $\hat{I}_{\text{AC}} = 10\,\text{A}$, which results in a fundamental output voltage of about $V_{\text{out,1}} = 330\,\text{V}$. Thus, the converter is feeding about 1.65 kW to the grid. The phase shift angle φ between the grid voltage V_{AC} and I_{AC} is about 16.5°, leading (over excited). This corresponds to a power factor of about $\cos(\varphi) = 0.96$. Figure 9a shows that, due to the feedback of the capacitor voltages, the discrete output voltage levels are properly modulated while altering the switching-state combinations. Thus, the current *THD* becomes about 3.28 %. On the contrary, when using the sensorless approach, the capacitor voltages slightly deviate during the operation. This is due to the fact that the nonlinear effects, such as the voltage drop across the IGBTs, the different self-discharge rates or the dead-time, are neglected during the offline generation of the optimal switching-state combinations. Thus, the discrete output voltage levels are slightly distorted while altering the switching-state combinations. This in turn results in an increased current *THD* of about 4.58 %.

As described in the IEEE standard 519-2014 [53], "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems", a maximum current *THD* of up to 20 % (depending on the connection point's Thévnin impedance) and up to 5 % is recommended for power consuming loads and power generating units, respectively. Consequently, the suggested control approach, including its sensorless variant, achieved a power-system-compliant current *THD* quality (<5 %).

Moreover, Figure 10a,b depict the harmonic components of the in Figure 9a,b depicted voltage and current waveforms, respectively. The depicted inset-figures in Figure 10a,b depict the harmonic components of the voltage and current waveforms in relation to their corresponding fundamental component and, in addition, the permissible, relative limits of the current harmonics according to the IEEE standard 519-2014 [53] are depicted by the green dashed line. All measured current harmonics comply with the specified limits. For both cases, with and without the sensing of the capacitor voltages, the third harmonic current component is the largest. Thus, the current *THD* value THD_{I} is mainly driven by the third harmonic, which is caused by the third harmonic component of the inverter output voltage. Consequently, to improve the current quality further, it might be reasonable

to implement a harmonic reduction technique, such as presented in [54,55] or [56], to decrease the third harmonic current component. Furthermore, triplen harmonics, such as the third harmonic, would not cause any currents if the inverter would be operated in an ungrounded three-phase system.

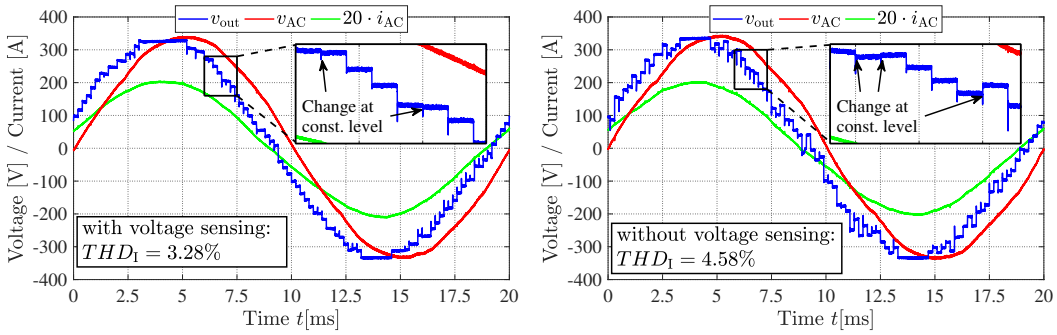


Figure 9. Measured operation of 33-level asymmetric MLC, controlling a grid current of $\hat{I}_{AC} = 10\,A$, (**a**) with and (**b**) without sensing of the capacitor voltages.

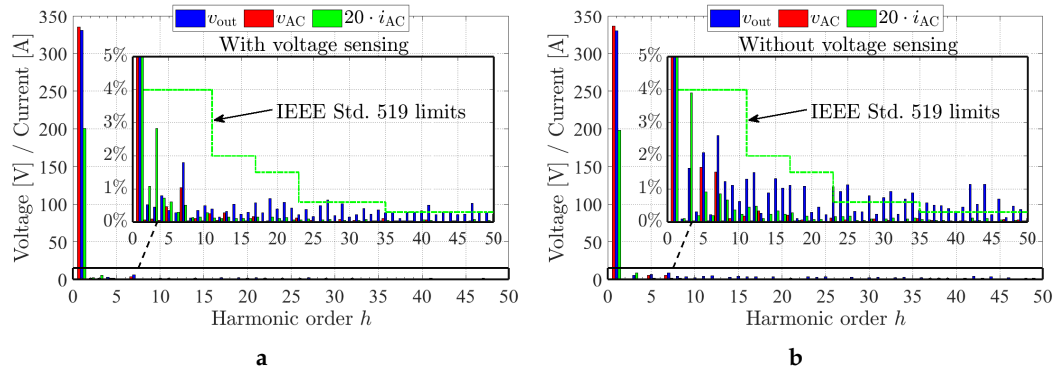


Figure 10. Harmonic components of measured voltage and current waveforms given in Figure 9, (**a**) with and (**b**) without sensing of the capacitor voltages.

7. Conclusions

Based on the concept of the weighted *THD* of MLIs' output voltage waveform, it was shown that a grid-tied (50 Hz) MLI with 33 discrete output voltages levels, operated with NLC, can presumably achieve a similar current *THD* as a single-phase H-bridge converter operated with a switching frequency of 25 kHz (three-level PWM). To utilize this advantage, binary asymmetric voltage levels can be used for MLIs' floating capacitor modules to reduce the number of required H-bridge modules.

This paper presented a novel capacitor voltage balancing approach applicable for cascaded multilevel converters with only one DC supply per phase and asymmetric capacitor voltages, tiered by a factor of two (binary asymmetric). Using a simple one-step ahead MPC approach, an optimal switching-state combination is mathematically determined among all redundant switching combinations to balance the capacitor voltages as quickly as possible. Furthermore, using the suggested optimal one-step ahead MPC approach, a series of offline calculated switching-state sequences for each discrete output voltage level can be used as lookup tables to operate the MLC without actually measuring (sensorless) the capacitor voltages. Using a Lyapunov function candidate, which is based on the energy stored in the grid filter's inductor and the H-bridges' capacitors, and considering LaSalle's invariance principle, the proposed sensorless control approach is asymptotically stable, and thus, the capacitor voltages and the grid current converge over time to their desired references.

To experimentally verify the effectiveness and the stability of the presented one-step

ahead balancing algorithm and its sensorless variant, a laboratory converter with four H-bridge stages, ideally achieving 33 discrete output voltage levels, was operated in grid-tied mode. Using a charging resistor during startup, the capacitor voltages converge to their desired reference levels, whereas the required charging time was increased from 2.2 s to 20 s when using the suggested sensorless control approach. The converter was operated with a sampling frequency of 5 kHz, which resulted in an actual switching frequency of 950 Hz and 2 kHz for the NPC stage and the individual H-bridge modules, respectively. For the chosen operating point ($\hat{I}_{\mathrm{AC}} = 10$ A) of the setup, the presented sensorless approach achieved a current $THD\ THD_{\mathrm{I}}$ of about 4.58%, which is slightly increased in comparison to 3.28% when operating the converter with the voltage sensors. Nonetheless, it was verified that the suggested sensorless approach is asymptotically stable and can be used in practice, although the dynamic response of the system and the output current quality is enhanced when using the voltage sensors.

So far, only the active power capability of the sensorless approach was considered. Thus, in a future work, the algorithm could be extended to control also the reactive power.

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