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# Graphene FET on diamond for high-frequency electronics

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**Abstract**—Transistors operating at high frequencies are the basic building blocks of millimeter-wave communication and sensor systems. The high charge-carrier mobility and saturation velocity in graphene can open way for ultrafast field-effect transistors with a performance even better than what can be achieved with III-V-based semiconductors. However, the progress of high-speed graphene transistors has been hampered by fabrication issues, influence of adjacent materials, and self-heating effects. Here, we report on the improved performance of graphene field-effect transistors (GFETs) obtained by using a diamond substrate. An extrinsic maximum frequency of oscillation  $f_{max}$  of up to 54 GHz was obtained for a gate length of 500 nm. Furthermore, the high thermal conductivity of diamond provides an efficient heat-sink, and the relatively high optical phonon energy of diamond contributes to an increased charge-carrier saturation velocity in the graphene channel. Moreover, we show that GFETs on diamond exhibit excellent scaling behavior for different gate lengths. These results promise that the GFET-on-diamond technology has the potential of reaching sub-terahertz frequency performance.

**Index Terms**—Diamond, field-effect transistors, graphene, maximum frequency of oscillation, MGFETs, optical phonons, saturation velocity, transit frequency.

## I. INTRODUCTION

Graphene is a 2D material with unique electrical properties such as extremely high charge-carrier velocity useful for transit types of devices [1]. There has been extensive research and progress on high-frequency graphene electronics since the first top-gated graphene field-effect transistor (GFET) was demonstrated in 2007 [2]. In 2012, excellent GFET performance with intrinsic transit frequencies above 400 GHz was achieved for a 67-nm gate length GFET [3]. However, this excellent performance was not matched by the maximum frequency of oscillation that lagged considerably due to non-negligible gate resistances.

In GFETs, the maximum frequency of oscillation is in part limited by poor drain current saturation which results in a non-negligible drain output conductance [4]. In 2016, an extrinsic transit frequency ( $f_T$ ) of 50 GHz and a maximum oscillation

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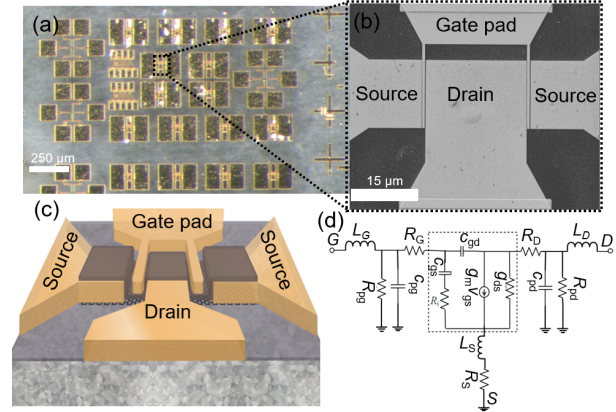


Fig. 1. Views of top-gate, dual-channel, high-frequency GFET on single crystal diamond substrate: (a) Photograph of the test chip, (b) SEM image, (c) schematic cross-sectional view, (d) small-signal equivalent circuit and dashed region indicates the intrinsic transistor elements.

frequency ( $f_{max}$ ) of 40 GHz was achieved for a gate length of 200 nm using quasi-freestanding bilayer epitaxial graphene grown on a SiC (0001) substrate [5]. Recently, using an improved fabrication process for CVD GFETs, Bonmann *et al.* demonstrated an extrinsic  $f_T$  of 34 GHz and a matching  $f_{max}$  of 37 GHz for 500-nm GFETs with promising scaling behaviour [6]. In order to minimise the output conductance it is essential to minimize the number of charge carriers not induced by the field such as carriers due to contaminants and traps in the adjacent materials, or carriers induced by self-heating.

Another performance-limiting factor is the influence on the charge-carrier velocity due to optical-phonon scattering with the materials surrounding the graphene channel. Hence, surrounding materials with high optical-phonon energies are preferred since there is a direct correlation between the charge-carrier velocity and the transit frequency as confirmed by ref [7].

In this work, we utilize both the high surface optical phonon energy and the high thermal conductivity of diamond as a substrate to increase the GFET performance. A record high extrinsic  $f_{max}$  of 54 GHz was achieved for a top-gated GFET on a single-crystal diamond substrate. We estimate the charge-carrier saturation velocity being as high as  $3.2 \cdot 10^7$  cm/s. Finally, we show that the high-frequency performance scales with the gate length, which indicates that GFETs on diamond have the potential of reaching sub-terahertz frequencies.

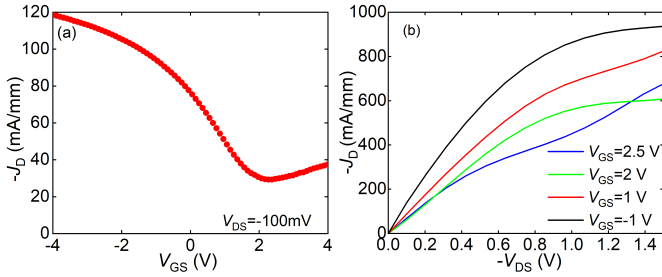


Fig. 2. GFET transfer characteristics (a) and output characteristics. (b) GFET geometry  $L_g = 0.5 \mu\text{m}$ ,  $W = 30 \mu\text{m}$ .

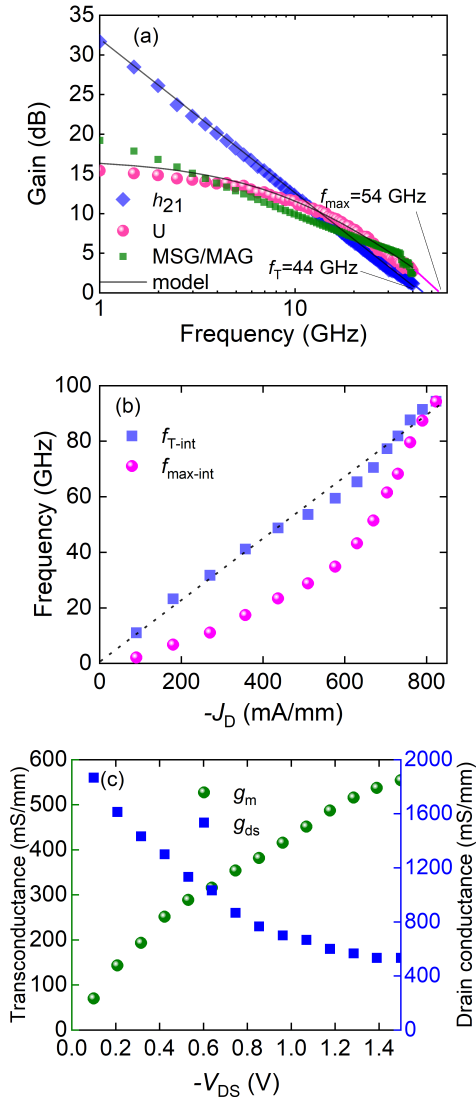


Fig. 3. Graphs showing (a) small-signal current gain  $h_{21}$ , maximum stable gain/maximum available gain (MSG/MAG), and Mason's unilateral gain  $U$  versus frequency obtained at  $V_{GS} = 1 \text{ V}$  and  $V_{DS} = -1.5 \text{ V}$ . Extrapolated extrinsic transit and maximum oscillation frequencies of 44 and 54 GHz, respectively, are obtained. Solid lines are obtained from the  $S$ -parameters simulated using small-signal equivalent circuit analysis. (b) Intrinsic transit and maximum-oscillation frequencies versus drain current density, (c) normalized small-signal conductances  $g_m$  and  $g_{ds}$  versus drain voltage.

## II. METHODS

Top-gated dual-channel RF GFETs were fabricated on a high-quality free-standing single-crystal diamond substrate. The commercially available diamond substrate was homoepitaxially grown in the (100) direction using chemical vapor deposition (CVD) by Element Six Ltd [8]. Fig. 1(a) shows an optical micrograph of a set of GFETs with gate lengths ( $L_g$ ) varying from  $0.5 \mu\text{m}$  to  $2 \mu\text{m}$  and a total gate width of  $30 \mu\text{m}$ . Fig. 1(b) shows a SEM image of a  $0.5 \mu\text{m}$  two-finger GFET. For illustration, Fig. 1(c) shows a three-dimensional view of the GFET layout. As a first step of the fabrication process, monolayer CVD graphene was transferred on to the diamond substrate, followed by deposition of a 5-nm thick  $\text{TiO}_2/\text{Ti}$  protection layer for avoiding contact between the electron-beam resist defining the source/drain areas and the graphene. After wet-etch removal of the protection layer in the source/drain resist openings,  $\text{Ti}/\text{Pd}/\text{Au}$  (1 nm/15 nm/285 nm) was deposited and source/drain contacts were fabricated using lift-off. The use of a protection layer is important for obtaining a clean metal/graphene interface and a low contact resistance. Next, the graphene mesa was defined. After removal of the remaining protection layer from the channel area, the gate dielectric stack was formed by a 5-nm thick thermally oxidized  $\text{Al}_2\text{O}_3$  seed layer and an 18-nm thick  $\text{Al}_2\text{O}_3$  top layer deposited by atomic layer deposition. The gate fingers, the gate pad, and the source/drain pads were formed by deposition of a  $\text{Ti}/\text{Au}$  (100 nm/300 nm) layer. All patterns were defined using electron-beam lithography.

For GFET characterization, transfer and output characteristics were obtained using a Keithley 2612B dual-channel source meter. High-frequency  $S$ -parameters were measured up to 40 GHz using an Agilent N5230A network analyzer. Two-port open-short-load-through calibration was performed using a standard calibration chip prior to the  $S$ -parameter measurements. De-embedding and extraction of the small-signal equivalent-circuit elements was performed based on the method described by Dambrine *et al.* [9]. Special test structures were included to find the pad capacitances and inductances from the  $S$ -parameter measurements. For analysing the GFET high-frequency performance, the small-signal equivalent circuit shown in Fig. 1(d) was used.

## III. RESULTS AND DISCUSSIONS

Fig. 2 shows the GFET transfer and output characteristics indicating typical GFET behavior. The  $J_D$  vs.  $V_{DS}$  curve obtained for  $V_{GS} = 1 \text{ V}$  shows the conditions under which the high-frequency performance was measured. Fig. 3 summarizes the measurement results obtained for the same GFET biased for maximum gain. First, the frequency-dependent current gain ( $h_{21}$ ), the Mason's unilateral power gain ( $U$ ), and the maximum stable gain/maximum available gain (MSG/MAG) obtained from the  $S$ -parameters are shown in Fig. 3(a). An extrinsic  $f_T$  as high as 44 GHz and an extrinsic  $f_{max}$  as high as 54 GHz are indicated by the figure. To the best of our knowledge, this is the highest reported extrinsic performance of top-gated CVD GFETs so far [6], [7], [10]–[13]. Fig. 3(b) shows an almost linear relationship between the

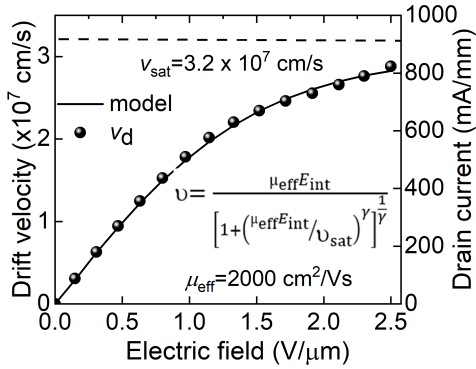


Fig. 4. Charge-carrier velocity (left axis) versus intrinsic electric field along the channel derived from the drain current density  $J_D$  vs.  $E_{int}$  (right axis) by assuming a constant charge-carrier concentration  $n=1.8 \cdot 10^{12} \text{ cm}^{-2}$  obtained from the slope of the  $f_{T-int}$  vs  $J_D$  graph shown in Fig. 3b. The Caughey-Thomas model [14] (solid line) with  $\gamma=3$  was used to estimate the saturation velocity (dashed line).

intrinsic transit frequency  $f_{T-int}$  and the drain current density  $J_D$ , indicating a practically constant charge-carrier density  $n$  throughout the whole drain bias range (0 to 1.5 V). This conclusion is based on the simple first-order assumption of an intrinsic transit frequency  $f_{T-int} = v_d / (2\pi L_g)$  and a drain current density  $J_D = qnvd$ , where  $v_d$  is the drift velocity, and  $q$  is the elementary charge. Based on these assumptions an effective charge carrier concentration  $n = 1.8 \cdot 10^{12} \text{ cm}^{-2}$  was obtained. Furthermore, the assumption of a constant charge-carrier density leads to the conclusion that the charge-carrier drift velocity profile can be obtained not only from the  $f_{T-int}$  vs.  $V_{DS}$  (as in previous work [7]) but also directly from the output characteristic  $J_D$  vs.  $V_{DS}$ . Finally, we can conclude that the effect of self-heating, typically resulting in an increasing charge-carrier density, is sufficiently low due to the high thermal conductivity of the diamond substrate.

From the broadband  $S$ -parameter measurements, the bias-dependent small-signal equivalent circuit parameters  $g_m$ ,  $g_{ds}$ ,  $C_{gs}$ , and  $C_{gd}$  were extracted and normalized by the gate width. The values of  $C_{gs}$  and  $C_{gd}$  are  $500 \pm 50 \text{ fF/mm}$ ,  $450 \pm 50 \text{ fF/mm}$ , respectively, and are almost constant across the drain bias range. Figs. 3(c) shows conductances  $g_m$  and  $g_{ds}$  versus the extrinsic drain voltage  $V_{DS}$ . The observed increase in transconductance  $g_m$  and decrease in drain conductance  $g_{ds}$  with  $V_{DS}$  are the two main factors for the enhanced high-frequency performance of these devices. Other extrinsic circuit elements such as the pad inductance ( $L_G = 13.8 \text{ pH}$ ,  $L_S = 1.6 \text{ pH}$ ,  $L_D = 5 \text{ pH}$ ), source/drain resistance ( $R_S/R_D = 23 \text{ } \Omega$ ), gate resistance, ( $R_G = 8 \text{ } \Omega$ ), parasitic pad capacitances ( $C_{PG} = 15 \text{ fF}$ ,  $C_{PD} = 4 \text{ fF}$ ), and parasitic pad resistances ( $R_{pad} = 21 \text{ k}\Omega$ ) are assumed to be bias-independent. Typically, due to zero-bandgap in monolayer graphene, GFETs reveal a linear output characteristic without drain current saturation resulting in a relatively high  $g_{ds}$  which has an adverse impact on the power gain i.e., limiting the  $f_{max}$ . In this work, high current density due to high charge carrier velocity and significant drain current saturation due to velocity saturation are observed and verified by the drain current modeling. The drain current saturation

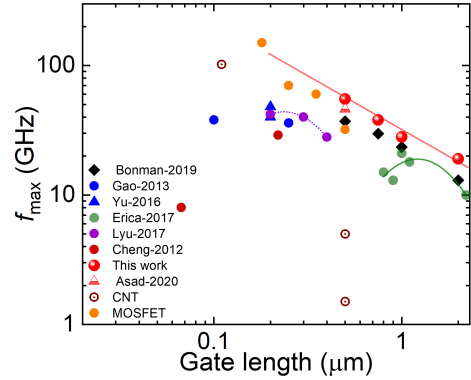


Fig. 5. Maximum frequency of oscillation ( $f_{max}$ ) versus gate length ( $L_g$ ). Solid red circles represent data from this work and the solid line showing a  $1/L_g$  dependence demonstrates the device scaling behavior. Also shown, for comparison, is data from GFETs on CVD, exfoliated and epitaxial graphene on silicon and SiC substrates [3], [6], [7], [10], [13], [15], from carbon nanotube FETs [16], [17] and from MOSFETs of similar gate lengths [18]–[20].

results in low  $g_{ds}$  and, thus enhanced  $f_{max}$ . Most promising way of increasing the high-frequency performance of GFET is by increasing the  $g_m$ , which is proportional to the  $v_d$ . The transconductance  $g_m$  shown in Fig. 3(d) increases with the  $V_{DS}$  and shows signs of saturation at higher field.

Fig. 4 shows the charge-carrier velocity found from the dependence of the drain current on the intrinsic drain field. The saturation velocity  $v_{sat}$  was derived by using the Caughey-Thomas velocity model [14] assuming a constant effective charge-carrier density – as previously concluded from the almost linear relationship between  $f_T$  versus  $J_D$  across the drain voltage range shown in Fig. 3(b). The  $v_{sat}$  in the diamond GFET is estimated being as high as  $3.2 \cdot 10^7 \text{ cm/s}$ . For comparison, the  $v_{sat}$  in an hBN-encapsulated graphene Hall-bar test structure was reported to  $5 \cdot 10^7 \text{ cm/s}$  [21].

To demonstrate the future prospects of the diamond GFET technology, the extrinsic performance of GFETs for different gate lengths is compared with published results in Fig. 5. In this work, the performance follows the solid trendline  $1/L_g^{0.9}$ , typical for Si-MOSFET and HEMT technologies [4], which indicates a good scaling behaviour. For instance, we foresee that  $f_{max} > 100 \text{ GHz}$  could be achieved for 200-nm GFET devices. The main improvements in the high-frequency performance and in the scaling behavior of the extrinsic  $f_{max}$  are mainly attributed to a higher carrier velocity, improved current saturation, and reduced effects of self-heating.

#### IV. CONCLUSIONS

In summary, the potential of top-gated graphene field-effect transistors on diamond substrate has been demonstrated. Substantial improvements in scaling behaviour and in maximum frequency of oscillation have been achieved due to the unique properties of diamond such as high surface-optical-phonon energy and high thermal conductivity when being used as a substrate. To reach the full potential of GFETs on diamond, both material quality and fabrication processes must be improved to achieve higher charge-carrier mobilities and saturation velocities.

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