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## **The H2020-SPACE-SIPHODIAS project: Space-grade optoelectronic interfaces for photonic digital and analogue very-high-throughput satellite**

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## The H2020-SPACE-SIPHODIAS Project: Space-grade Opto-electronic Interfaces for Photonic Digital and Analogue Very-High-Throughput Satellite payloads

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### ABSTRACT

The EU-SIPhDiAS project deals with the development of critical photonic building blocks needed for high-performance and low size, weight, and power (SWaP) photonics-enabled Very High Throughput Satellites (VHTS). In this presentation, we report on the design and fabrication activities during the first year of the project concerning the targeted family of digital and microwave photonic components. This effort aims to demonstrate components of enhanced reliability at technology readiness level (TRL) 7. Specifically, with respect to microwave photonic links, we report: (i) the design of Ka and Q-bands analogue photodetectors that will be assembled in compact packages, allowing for very high bandwidth per unit area and (ii) on the design of compact V-band GaAs electro-optic modulator arrays, which use a folded-path optical configuration to manage all fiber interfaces packaged opposite direct in-line RF feeds for ease of board layouts and mass/size benefits. With respect to digital links, we report on the development of 100 Gb/s (4 x 25 Gb/s) digital optical transceiver sub-assemblies developed using flip-chip mounting of electronic and opto-parts on a high-reliability borosilicate substrate. The transceiver chipset developed specifically for this project refers to fully-custom 25 Gb/s radiation hard (RH) VCSEL driver and TIA ICs designed in IHP's 130 nm SiGe BiCMOS Rad-Hard process.

**Keywords:** VHTS, photonic payload, VCSEL driver, TIA, digital transceiver, on-board optics, Ka-band photodetectors, electro-optic modulator arrays, BiCMOS,

### 1. INTRODUCTION

Several approaches have been pursued for broadband satellite payloads featuring multi-beam antennas and hundreds of channels to receive, route and transmit. Payloads have evolved from the old “bent-pipe” repeater concept to more advanced analogue microwave sub-systems or to digital processor-based solutions. Payloads of the latter type

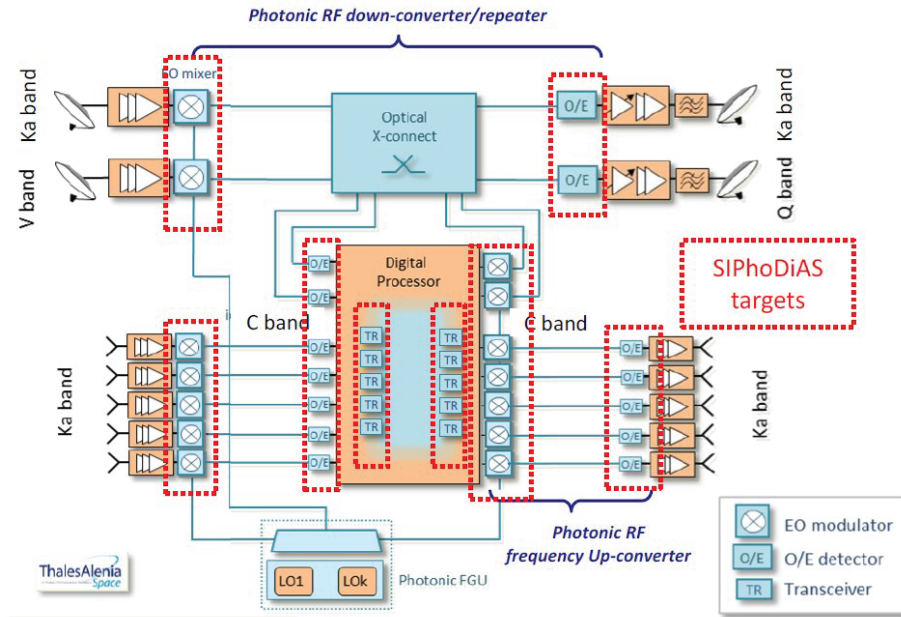


Figure 1: Overview of a photonic payload and the SIPhoDiAS targeted components: digital transceivers (TR), opto-electronic detectors (O/E), electro-optic modulator arrays (mixer symbol).

incorporate an increasing amount of digital signal processing (DSP) equipment for filtering, switching and/or regenerating telecom signals. A combination of the above architectures is under consideration. It can be typically referred to as hybrid analogue/digital payload. Combining analogue and digital sub-systems could provide the large capacity and flexibility required for future VHTS systems. Under increasing capacity and stringent size, weight, and power (SWaP) requirements, a technology switch that relies on photonics is more and more embraced.

Thales Alenia Space has been the first to introduce optical interconnects in a commercial digital payload [1] and this opens the opportunity for photonics penetration in every part of the satellite payload. Figure 1 shows the conceptual architecture of such a photonics-enabled hybrid payload in Ka/Q/V bands with multi-feed antennas and active array antennas, with broadband routing, performed by a photonic RF repeater sub-system, and flexible channelization as well as bandwidth allocation by an optically-interconnected, high-throughput digital processor. The dotted blocks indicate the areas where the critical opto-electronic (O/E) interfaces are located. To deliver future high-performance photonics-enabled VHTS, these interfaces - transceivers, modulators and photodetectors are deployed in the highest volumes and interconnect equipment at the edge or within the payload. Their current performance in speed, bandwidth, reliability and, most importantly, in size and power consumption can be significantly enhanced. SIPhoDiAS [2] aims to advance these components performance, and at the same time, enhance their reliability demonstrating parts at technology readiness level (TRL) 7.

In this presentation, we report on the design and fabrication activities on the developed family of digital and microwave photonic components. With respect to microwave photonic links, in Section 2, we report the design of Ka and Q-bands analogue photodetectors that will be assembled in compact packages targeting more bandwidth per unit area. In Section 3, we report the design of compact V-band GaAs electro-optic modulator arrays, which use a folded-path optical configuration to manage all fiber interfaces packaged opposite direct in-line RF feeds for ease of board layouts and mass/size benefits. In Section 4, we present the development of 100 Gb/s (4 x 25 Gb/s) borosilicate-based digital photonic transceiver sub-assemblies, featuring flip-chipped rad-hard VCSEL drivers and TIAs designed in IHP's SG13RH (Rad-Hard) 130nm BiCMOS process, fully-custom developed for the SIPhoDiAS project.

## 2. KA AND Q-BANDS ANALOGUE PHOTODETECTORS

Albis Optoelectronics develops the high-speed, hermetic photodetector modules designed for analogue applications in Ka- (17.3-20.2 GHz) and Q-band (37.5-42.5 GHz). The package is optimized with regards to reduced size, weight and power (SWaP) required for spaceborne applications. The estimated weight of the photodetector is approximately 8 g excluding the RF connector and the fiber pigtail. The proposed package design is shown in Figure 2 with an optical feedthrough on the left side and the K-connector on the right side of the package. The analogue photodetector includes an internal bias-T, which is connected to separated pins for the DC and ground connection on the backside of the package. Inside the package a backside illuminated photodiode with a monolithically integrated lens – showed in Figure 3 – is used. The photodiode PD40X1 is flip-chip mounted onto a ceramic carrier that integrates the required matching circuit for broadband Ka- and pass-band Ka- and Q-band matching. The alignment of the photodiode is achieved by a 45° angle fiber pigtail, which is terminated with an FC/APC connector. The integrated backside lens provides additional alignment tolerances and optimized optical coupling efficiency, which enables a high responsivity.

Measurements of the optical coupling from a butt coupled single mode fiber (SMF) to the photodiode with integrated backside lens show how the optical coupling is greatly simplified. An illustration of the optical path used in the measurements is depicted in Figure 3 on the left side. For the responsivity scan measurements, the light coming out of a butt coupled SMF enters the photodiode backside with normal incidence while the fiber-to-lens distance ( $d$ ) was varied. The graphs in Figure 4 on the right side show the responsivity scan across the x-direction through the lens center. Lateral displacement of the light being emitted from the fiber with respect to the lens center (by misalignment of the photodiode during assembly) should have no significant impact on the optical coupling, since the -0.2 dB responsivity plateau is approximately 35  $\mu\text{m}$  wide at a distance of  $d = 25 \mu\text{m}$ . The expected responsivity of the lensed photodiode at 1550 nm, excluding coupling losses, is 0.8 A/W.

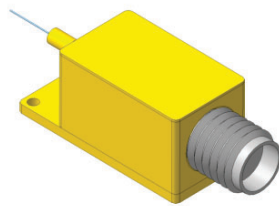


Figure 2: Conceptual design of the PD module with K-connector.

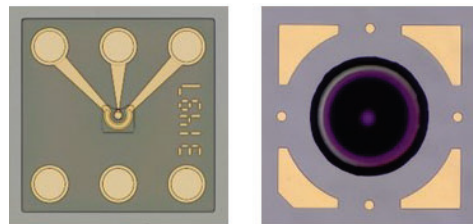


Figure 3: Photograph of the Albis photodiode chip PD40X1 showing the topside electrical contact pads and the backside with the monolithically integrated lens.

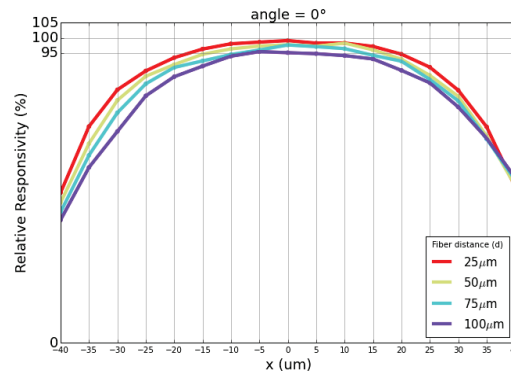
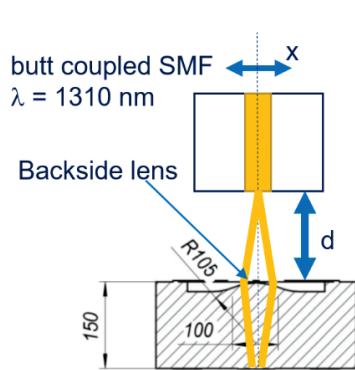


Figure 4 Left: Illustration of the optical path used in the responsivity scan measurements. The sketch shows the placement of the fiber tip with respect to the photodiode backside. Right: Responsivity scan measurements with varying fiber-to-lens distance. The graphs show the relative responsivity in x-direction through the lens center.

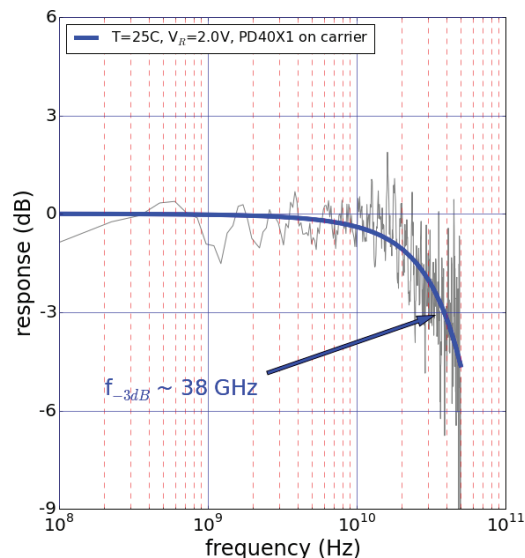


Figure 5: Frequency response measurement.

The electro-optical characterization of the photodiode is performed on a ceramic carrier. Figure 5 presents the frequency response at room temperature with a bias voltage of 2V. At approximately 38 GHz signal frequency the response has dropped by 3 dB. The bandwidth of the photodiode is expected to meet the requirements of a Ka- and Q-band packaged photodetector module once the electrical RF matching circuit will be included.

### 3. 50 GHZ GALLIUM ARSENIDE ELECTRO-OPTIC MODULATOR ARRAYS

Modulators based on gallium arsenide have clear advantages in exploiting the enormous data capacity of multiplexed optical links, as they progress towards Q/V bands. Electro-optic modulators are viewed as a Critical Space Technology for microwave photonic payloads, with increasing interest in frequencies of 50GHz and higher by the European Space Agency [3].

The environmental credentials of gallium arsenide in the GaAs/AlGaAs III-V semiconductor material system are well known; the large semiconductor bandgap yields environmental stability and a useful degree of radiation tolerance [4]. This makes it a natural choice for space-borne systems, with many desirable properties for RF devices, which must survive and operate in harsh environments. Traveling-wave electro-optic modulators in GaAs have similar linearity to the better-known lithium niobate devices but can exhibit higher bandwidths and lower drive-voltages within a significantly more compact footprint, which is half the size and weight, as well as offering enhanced bias stability. Folding of the optics within the device allows the fiber connections to be managed at one end, reducing the overall volume occupied.

The folded topography (see Figure 6) has other advantages once arrays of modulators are contemplated since it allows symmetric RF connections which provide uniform high frequency performance across the channels and no limit to the size of the array. It is possible to arrange four modulator arrays in the same size package as the base modulator, giving significant advantages for satellite applications. Using fiber array interfaces, the package width is limited by the RF connectors and not by the devices which remain the same length for all sizes of arrays. The fiber interfaces for arrays provide new challenges since there is a need to use polarization maintaining fibers. The SIPhoDiAS project is developing these array fiber interfaces using silicon v-groove mounting blocks which provide the precision necessary for managing multiple parallel fibers.

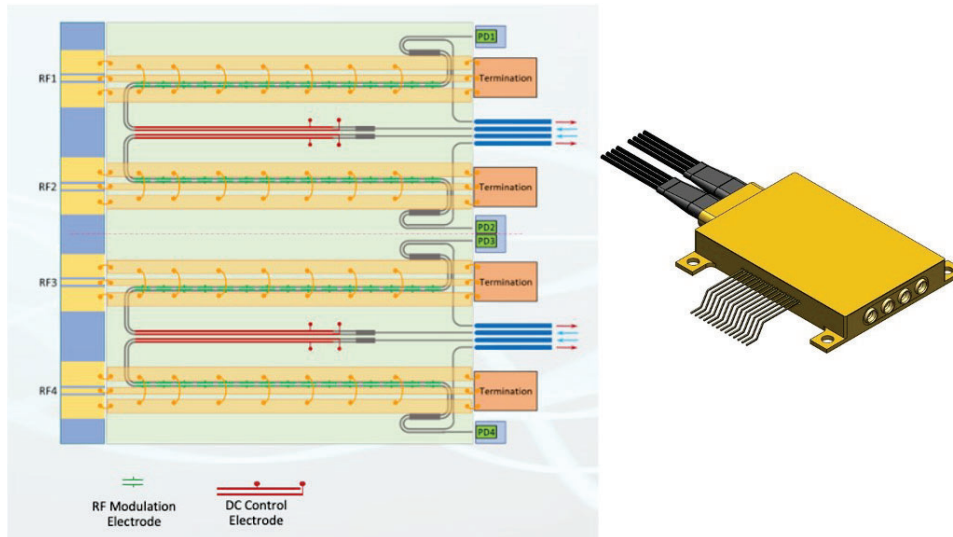


Figure 6: Folded GaAs MZM schematic showing parallel, symmetric array interfaces.

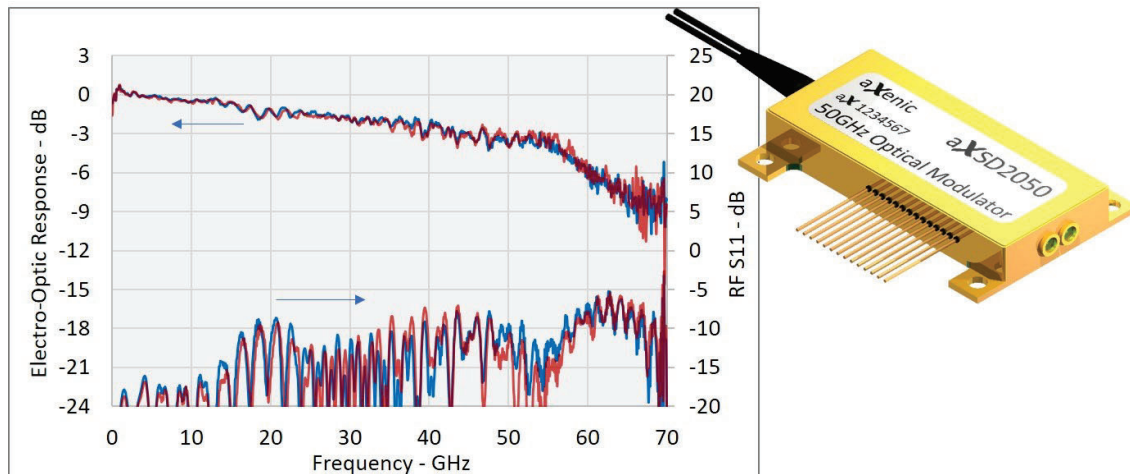


Figure 7: Measured electro-optic RF characteristics for both I and Q channels of a 50 GHz folded-path GaAs IQ modulator module.

As a precursor to the arrays, we have demonstrated IQ modulators which are dual parallel modulators but with a single input and output fiber. The performance is shown in Figure 7 where a bandwidth of nearly 45 GHz has been achieved in both channels in a device with DC  $V_{\pi}$  of 5 V and fiber-to-fiber loss of less than 7 dB. The target performance of the project is to achieve arrays of devices with improved bandwidth capability, lower loss and drive voltage.

#### 4. DIGITAL OPTICAL TRANCEIVER

The increasing data rates for interconnect applications, driven mainly by the demand for scaling datacenters, create challenging conditions for signal integrity on the host PCBs. Optical interconnects are becoming the standard choice

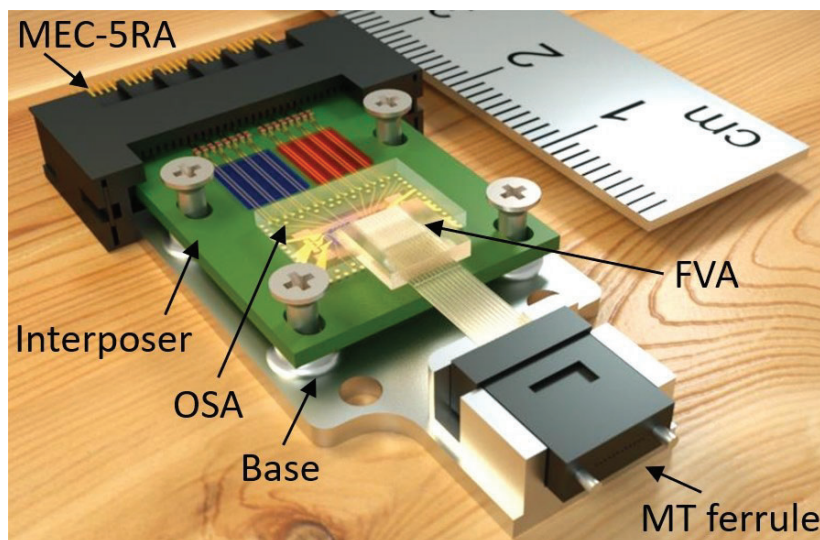


Figure 8: CAD design of the digital transceiver package (open-lid) interfacing a processor ASIC.

even for short ranges of interconnect lengths as in inter-board links. In systems such as digital payloads, where the density of I/Os becomes important as well, mid-board embedded optics solutions provide the form factor required that can enable populating a host PCB to reach the required capacity.

The digital transceiver chipset developed for SIPhoDiAS refers to 850 nm multimode fiber coupled rad-hard VCSEL driver and TIA receiver circuits hosted on a mid-board optical sub-assembly interfacing a core digital processor. The first generation of the project reported here aims to deliver an aggregate data rate of 100 Gbps featuring 4 channels of 25 Gb/s for each chip.

The mid-board module designed for the project is shown in Figure 8. The mid-board electrical interface is the Samtec MEC-5RA connector, which is a pluggable solution. It supports up to 56 Gb/s PAM4 modulation and is compatible with the COBO standard for high-speed board-mountable optical transceivers. It helps maintain a small form factor as well as a future-proof scalability of electrical outputs without significantly impacting size and weight. This design keeps the RF tracks of the Interposer PCB to a single plane and is better optimized for retaining signal shape & strength.

The interposer hosts a borosilicate carrier Optical Sub-Assembly (OSA) for the transceiver ICs and provides room to accommodate optionally a retiming circuit. The borosilicate carrier acts as a substrate for electrical routing leading to the flip-chipped electronics through stud-bumps, but in the same time, it provides the means for waveguiding light from the VCSEL or to the TIA IC connected to a Fiber V-groove Assembly (FVA). The package optical interface is an MT ferrule, which holds the eight multi-mode fibers. The transceiver is sized 17 mm x 38.42 mm x 7.2 mm with a targeted temperature range from -40 °C to 85 °C.

The VCSEL and photodiode used for the digital transceivers were selected amongst commercially available solutions after performance benchmarking. The main criteria being performance and reliability. Electrical testing has revealed the performance characteristics while radiation testing is under way. The acquired VCSEL samples were characterized over a temperature range of 25 to 100 °C. IPV and bandwidth measurements indicate similar performance among vendors. The S21 measurements indicate that a ~14 GHz 3dB bandwidth at a typical bias current of 5mA could be attainable.

Optical simulations were performed to ensure the alignment tolerances within the module are understood. Figure 9 shows a Zemax simulation for the VCSEL. The alignment tolerance of the VCSELs indicated a variation of <0.1 dB coupling loss across, an acceptable lateral tolerance offset, as well as a negligible impact on coupling losses over short depth distances. Photodiode alignment was found to be more sensitive due to the small size of the PD aperture. A coupling loss increase of 0.5 dB was found over the same lateral offset as for the VCSEL simulations. The FVA to OSA coupling accuracy tolerance was also simulated. The VCSEL was modelled spatially as a Gaussian output, as although this is wider than the actual propagation, it will allow for more filling of higher order modes depending on the coupling

of the VCSEL. VCSEL angular distribution should be largely unaffected. For the PD side, the fiber output was represented by fully filled spatial modes (top hat distribution with cut off at  $\pm 25 \mu\text{m}$ ). Modelling using these assumptions, and considering light losses, the VCSEL nominal coupling was found to be 76.6%, corresponding to a loss of 1.16 dB. Nominal coupling of the photodiode was modelled at 74%, corresponding to a loss of 1.28 dB.

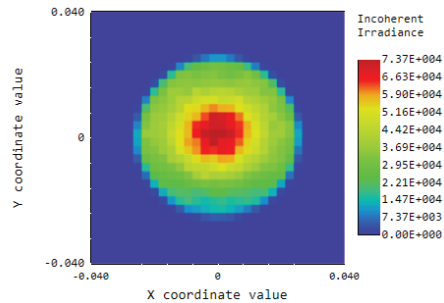


Figure 9: Zemax simulation result for the VCSEL alignment losses

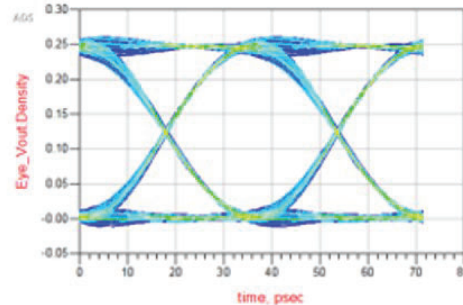


Figure 10: Eye diagram simulating the MEC5-RA connector performance for 28Gbps

The optical modelling was taken further to investigate the sensitivity tolerance of the alignment process. Epoxy thickness, pitch of fibers, offset at right angles to pitch, and fiber cut angle were measured.

It was found that the VCSEL underfills the fiber and the PD overfills the fiber, but for both components a threshold exists below which the effect of epoxy thickness on performance is negligible. There is a maximum of 0.1 dB loss when the epoxy is applied using ALTER UK standard assembly processes.

It was observed that when the loss in one component due to fiber cut angle decreases, the other increases. However, an optimum angle was found such that keeping the overall sensitivity as specified by the fiber supplier at  $\pm 0.3 \text{ }^\circ\text{C}$  is reasonable. It should be noted that both parts reach a maximum coupling value.

X-offset losses increase quadratically; the PD is more sensitive since it is a bigger spot at the target. Y-offset losses are asymmetric, as the beam must travel further when reflecting from the bottom of the fiber. Losses are symmetric for fiber tilt. By assembling to alignment tolerances set at ALTER, we can maintain a 0.1 dB sensitivity for both VCSEL & PD.

An overview of the implemented link is shown in Figure 11. Electrical EM modeling and simulations were performed throughout the design of the transceiver, including opto-part to IC interconnections, stud-bump performance, interposer design & electrical connector choice. The connector was found to present the bottleneck of performance. Without it, the signal path's insertion loss was found under -3.0 dB up to 40 GHz, with a mostly flat frequency response, but when included in the simulation, an insertion loss of less than -3 dB is exhibited up to 16 GHz.

The integrated rad-hard Driver and TIA circuits were designed in IHP's 130nm SiGe:C BiCMOS technology, and specifically in the SG13RH (Rad-Hard) process. The process features high speed SiGe HBTs with  $f_T / f_{max} = 250/340$  GHz that have been proven to be resistant to total ionizing dose (TID) levels up to 1.2 MRad. IHP's rad-hard digital library, which contains rad-hard triple modular redundancy flip-flops was used to integrate I/O cells and a digital control block for each design in the form of a Serial-to-parallel interface (SPI) core.

The modeling and measurement campaign for the opto-parts and the package has provided an opto-aware/package-aware IC design process, which targeted important optimizations to leverage the needed robustness with a low power consumption [5]. The multi-channel ICs submitted for fabrication feature 4 x 25 Gb/s targeted data rate, on-chip regulation and SPI control along with temperature sensing and wide range of tunability. The ICs are powered by a single 3.3 V supply and post layout simulations project to consume around a combined 6 mW/Gbps for nominal operation.

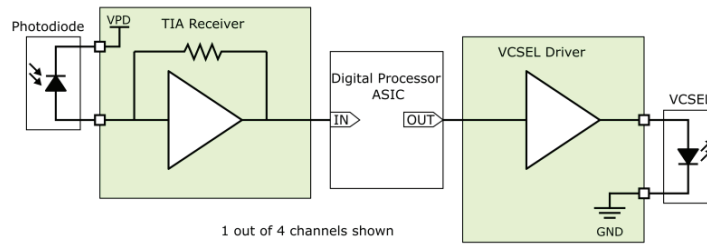


Figure 11: Overview of the digital transceiver deployment interfacing a processing ASIC.

## 5. CONCLUSIONS

In this presentation we are demonstrating the advances in the frame of the EU-SIPhoDiAS project. Critical photonic building blocks needed for high-performance and low size, weight, and power (SWaP) photonics-enabled Very High Throughput Satellites (VHTS) are developed. More specifically we report (i) a 8 g packaged, 0.8 W/A photodiode with a bandwidth of 38 GHz (ii) 45 GHz GaAs dual parallel I-Q electro-optic modulators with a fiber-to-fiber loss of less than 7 dB (iii) an on-board optics borosilicate-based transceiver module with a small form factor (17 mm x 38.42 mm x 7.2 mm), featuring pluggable connectors and targeting to host a chipset of custom designed 4 x 25 Gbps rad-hard VCSEL and TIA ICs (currently in fabrication stage) developed in IHP's BiCMOS 130nm Rad-Hard process node.

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