THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

InP High Electron Mobility Transistors for Cryogenic Low-Noise and Low-Power Amplifiers

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Abstract

The InAlAs/InGaAs/InP high-electron mobility transistor (InP HEMT) is the preferred low-noise device in cryogenic low-noise amplifiers (LNAs) operating at 5−15 K. Such LNAs are utilized in microwave and millimeter-wave detection in radio astronomy. In order to further reduce the noise level, a deeper understanding of the InP HEMT under cryogenic low-noise operation is necessary. In addition, InP HEMTs with very low dc power dissipation have recently become of interest due to power constraints when scaling quantum computing systems with large number of cryogenic LNAs.

This thesis presents progress in InP HEMT technology for cryogenic LNAs. Three areas are addressed: device scaling, dc power optimization, and electrical stability at cryogenic temperature. The InP HEMT optimization are discussed in terms of the epitaxial layer design, fabrication, dc, rf, and noise characteristics.

A 100 nm gate-length InP HEMT technology was developed by scaling of the barrier thickness. Despite increased gate leakage current, state-of-the-art cryogenic noise performance for a wide-band monolithic microwave integrated circuit (MMIC) LNAs was demonstrated with average noise temperature of 3.5 K and 6.3 K for the 0.3−14 GHz and 16−28 GHz designs, respectively.

The impact of barrier thickness and channel composition on the cryogenic noise temperature and dc power dissipation of the InP HEMT LNAs was studied. Through the barrier scaling, the HEMT achieved an improvement of transconductance to drain current ratio at low drain voltages, which enabled a reduction of the power dissipation to 112 μW with an average noise temperature of 4.1 K in a 4−8 GHz InP HEMT LNA. From a comparative study of $In_{0.65}Ga_{0.35}As$ and $In_{0.8}Ga_{0.2}As$ channels, the InP HEMT with lower indium channel content resulted in superior cryogenic noise performance.

The cryogenic stability of two-finger InP HEMTs was investigated. The InP HEMTs exhibited anomalous electrical behavior such as jumps in drain current and sharp peaks in transconductance. Three different design techniques were shown to mitigate the electrical instabilities associated with cryogenic operation. A cryogenic 24–40 GHz and a 28–52 GHz MMIC LNA based on the source air-bridge design technique for the two-finger InP HEMTs were demonstrated. The average noise temperature was 10.6 K and 10 K in the 24−40 GHz and 28−52 GHz LNAs, respectively. Both LNA designs demonstrated the lowest noise temperature reported so far for cryogenic MMIC LNAs for these frequency bands.

Keywords: cryogenic, InP high-electron mobility transistor (InP HEMT), low-noise amplifier (LNA), noise temperature, dc power dissipation, scaling, indium channel content, electrical stability.

List of Publications

Appended Publications

This thesis is based on the work contained in the following papers:

[A] **Eunjung Cha**, Giuseppe Moschetti, Niklas Wadefalk, Per-Åke Nilsson, Stella Bevilacqua, Arsalan Pourkabirian, Piotr Starski, and Jan Grahn,"Two-Finger InP HEMT Design for Stable Cryogenic Operation of Ultra-Low-Noise K- and Q-Band LNAs", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 65, No. 12, pp. 5171-5180, Dec. 2017, doi: 10.1109/TMTT.2017.2765318.

[B] **Eunjung Cha**, Niklas Wadefalk, Per-Åke Nilsson, Joel Schleeh, Giuseppe Moschetti, Arsalan Pourkabirian, Silvia Tuzi, and Jan Grahn,"0.3–14 and 16–28 GHz Wide-Bandwidth Cryogenic MMIC Low-Noise Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 66, No. 11, pp. 4860-4869, Nov. 2018, doi: 10.1109/TMTT.2018.2872566.

[C] **Eunjung Cha**, Niklas Wadefalk, Giuseppe Moschetti, Arsalan Pourkabirian, Jörgen Stenarson, and Jan Grahn,"A 300-μW Cryogenic HEMT LNA for Quantum Computing", *in IEEE MTT-S International Microwave Symposium*, Los Angeles, USA, Aug. 2020, doi: 10.1109/IMS30576.2020.9223865.

[D] **Eunjung Cha**, Niklas Wadefalk, Giuseppe Moschetti, Arsalan Pourkabirian, Jörgen Stenarson, and Jan Grahn,"InP HEMTs for Sub-mW Cryogenic Low-Noise Amplifiers", *IEEE Electron Device Letters*, Vol. 41, No. 7, pp. 1005-1008, Jul. 2020, doi: 10.1109/LED.2020.3000071.

[E] **Eunjung Cha**, Niklas Wadefalk, Giuseppe Moschetti, Arsalan Pourkabirian, Jörgen Stenarson, Junjie Li, Dae-Hyun Kim, and Jan Grahn,"InP HEMT Channel Design for Ultra-Low Power Cryogenic Low-Noise Amplifiers", *Manuscript*, 2020.

Other Publications

The following publications are not appended to the thesis, either due to contents overlapping with appended papers, or due to contents not related to the thesis.

[a] **Eunjung Cha**, Niklas Wadefalk, Giuseppe Moschetti, Arsalan Pourkabirian, Jörgen Stenarson, and Jan Grahn, "Impact of Indium Channel Content in InP HEMTs for Cryogenic C-Band Low Noise Amplifiers", accepted in *Compound Semiconductor Week*, 2020.

[b] **Eunjung Cha**, Giuseppe Moschetti, Niklas Wadefalk, Per-Åke Nilsson, Stella Bevilacqua, Arsalan Pourkabirian, Piotr Starski, and Jan Grahn, "Two-Finger InP HEMT Design for Stable Cryogenic Operation of Ultra-Low-Noise Ka-Band LNAs", in *IEEE MTT-S International Microwave Symposium*, Honolulu, Hawaii, 2017.

[c] Joel Schleeh, Giuseppe Moschetti, Niklas Wadefalk, **Eunjung Cha**, Arsalan Pourkabirian, Göran Alestig, John Halonen, Bengt Nilsson, Per-Åke Nilsson, and Jan Grahn, "Cryogenic LNAs for SKA band 2 to 5", in *IEEE MTT-S International Microwave Symposium*, Honolulu, Hawaii, 2017.

[d] Yulung Tang, Niklas Wadefalk, Jacob W Kooi, Joel Schleeh, Giuseppe Moschetti, Per-Åke Nilsson, Arsalan Pourkabirian, **Eunjung Cha**, Silvia Tuzi, and Jan Grahn, "Cryogenic W-band LNA for ALMA band 2+3 with average noise temperature of 24 K", in *IEEE MTT-S International Microwave Symposium*, Honolulu, Hawaii, 2017.

[e] **Eunjung Cha**, Arsalan Pourkabirian, Joel Schleeh, Niklas Wadefalk, Giuseppe Moschetti, Piotr Starski, Göran Alestig, John Halonen, Bengt Nilsson, Per-Åke Nilsson, and Jan Grahn, "Cryogenic low-noise InP HEMTs: A source-drain distance study", poster contribution in *Compound Semiconductor Week*, Toyama, Japan, Jun. 2016.

[f] **Eunjung Cha**, Arsalan Pourkabirian, Joel Schleeh, Niklas Wadefalk, Giuseppe Moschetti, Piotr Starski, Göran Alestig, John Halonen, Bengt Nilsson, Per-Åke Nilsson, and Jan Grahn, "InP HEMT With Noise Temperature below 1 K", presented in *Swedish Microwave Days*, Linköping, Sweden, Mar. 2016.

Thesis

As part of the author's doctoral studies, some of the work presented in this thesis has previously been published in [g]. Figures, tables and text in [g] might therefore be fully or partly reproduced in this thesis.

[g] **Eunjung Cha**, "InP High Electron Mobility Transistor Design for Cryogenic Low Noise Amplifiers", Thesis for the Degree of Licentiate of Engineering, Chalmers University of Technology, Sweden, 2018.

Contents

Chapter 1

Introduction

InAlAs/InGaAs/InP high-electron mobility transistors (InP HEMTs) have long provided superior low-noise amplification at microwave and millimeter-wave frequencies. Low-noise amplifiers (LNAs) operating at cryogenic temperatures, typically 5−15 K, are essential for detection arrays with a large number of receiving antennas in radio astronomy and deep-space communication. With LNAs in the first stage of the receiving system, the low-noise HEMT LNA is one of the key components to reduce the system noise.[1–9] Cryogenic LNAs based on InP HEMT technology have demonstrated state-of-the-art noise results of 1.6−1.8 K in 4−8 GHz,[3,10] 4.4 K in 0.5−13 GHz,[11] 11.4 K in 26−40 GHz,[5] and 13 K in 35−50 GHz.[6] The noise performance of the cryogenic LNA is largely determined by the minimum noise temperature of the transistor. Thus, in order to further improve cryogenic noise performance, a deeper understanding of the InP HEMT under cryogenic low-noise operation is necessary. This thesis presents advancements in InP HEMT technology for cryogenic LNAs in the microwave and millimeter-wave frequencies. The work is divided into scaling the transistor, optimizing the low-noise HEMT for low-power operation, and a solution for stable device operation at cryogenic temperatures.

For advances in the low-noise properties of the transistor, the device technology has been developed enhancing the cut-off frequency (f_T).[12] A traditional way to improve high-speed and low-noise performance is by scaling down the device.[12–15] However, scaling tends to increase the gate leakage current.[13,16] It is well-known that this is detrimental to the cryogenic noise properties, in particular at low frequencies.[3,12,17,18] The optimization of the InP HEMTs via scaling is thus not straightforward. Further research on the trade-off between scaling of the HEMT and the gate leakage current is necessary for advances in the noise performance at cryogenic temperatures.

One of the unexplored subjects of cryogenic InP HEMT technology is its potential for low-power consumption. In the recent demonstration of 54 qubit quantum processor, cryogenic 4–8 GHz InP HEMT LNAs were employed at the 4 K stage for qubit readout.[19] One single cryogenic LNA is required for every 5−10 qubits, and the dc power dissipation (P_{dc}) of the HEMT LNA is around several milliwatts.[3,19] For scaling quantum computing technology to the million qubit level, the dc power must be reduced considering integrating thousands of HEMT LNAs into a single cryogenic cooling system. This serves as motivation to minimize the dc power consumption of cryogenic InP HEMT LNAs with sufficient gain and noise temperature. Cryogenic SiGe HBT LNAs have been shown to operate at power levels in the low hundreds of microwatts,

and are therefore one promising candidate for quantum readout systems: cryogenic noise of 7−8 K with 26−30 dB gain at P_{dc} of only 300−580 μW have been demonstrated at 4−8 GHz.[20,21] A 4−8 GHz InP HEMT LNA with 7.2 K noise with 17 dB gain at P_{dc} of 100 μW was reported already in 2003.[10] In this thesis, it is shown that InP HEMTs can be optimized for cryogenic 4−8 GHz LNAs operating at almost 100 μW with much lower noise temperature.

A challenge for cryogenic low-noise HEMTs is electrical instability which is often more pronounced at cryogenic temperatures than at room temperature. Abnormal cryogenic HEMT operation has been reported in several studies.[17,22–27] The four-finger metamorphic HEMT (mHEMT) exhibited a sudden change in the drain current, and a significant reduction in gain at cryogenic temperatures.[26] Stabilization methods for four-finger devices were demonstrated by G. Moschetti *et al.*[26] and M. Varonen *et al.*[22] The two-finger device has also been shown to exhibit cryogenic anomalous behavior, which was reported already in 1986.[27] Reliable and reproducible cryogenic LNA operation can only be obtained when the HEMT operates in a stable manner at cryogenic temperatures. Therefore, cryogenic instability in two-finger InP HEMTs was investigated in this thesis for reliable LNA operation.

This thesis presents InP HEMT technology optimized for low-noise, low-power dissipation, and electrical stability at cryogenic temperature. In Chapter 2, a background to the noise model for the InP HEMT and a noise modeling method used in this thesis are described. In Chapter 3, the optimization of the InP HEMT technology for cryogenic LNA designs is presented. The technology will be discussed in terms of the epitaxial design and the fabrication process. In Chapter 4, the influence of InP HEMT scaling on the cryogenic noise performance up to 30 GHz is discussed. In Chapter 5, the InP HEMT technology developed for ultralow-power dissipation is presented. State-of-the-art noise results in the sub-mW 4−8 GHz cryogenic LNA are demonstrated, and the effect from indium content in the InP HEMT channel on cryogenic noise properties is followed. In Chapter 6, the electrical cryogenic instability in two-finger HEMTs and design techniques for stable cryogenic operation are presented. Finally, Chapter 7 summarizes the results of this thesis and provides an outlook for future work.

Chapter 2

Noise Modeling of the InP HEMT

Noise models for transistors are important for the physical interpretation of the device noise and for designing low-noise amplifiers. Model parameters representing noise properties of the device allow insight into the physical origin of various noise sources and their contributions to the total measured noise temperature.[28] In addition, the knowledge of temperature dependent noise properties is crucial to optimize the low-noise transistor for a certain operating temperature. This chapter presents a background to the noise model for the InP HEMT and a noise modeling method used in this thesis.

2.1 Noise parameters

The main noise sources in the microwave HEMT are thermal noise, shot noise, and hot-electron noise.[29] Any resistance shows current fluctuations caused by the thermal motion of the electrons, resulting in thermal noise. Since the thermal noise is proportional to the ambient temperature, cryogenic cooling effectively reduces this contribution to the total noise. The shot noise is important in structures where the current is controlled by a barrier. In the HEMT, the shot noise originates from the Schottky barrier under the gate. It is white over a wide range of frequencies, and is proportional to the gate current. The hot-electron noise is associated with kinetic processes in the conduction band, such as energy relaxation, intervalley transfer, and impact ionization, and the relevant frequency range is from 1 GHz to 1 THz.[29]

The Pospieszalski noise model is widely used for predicting noise parameters of the field-effect transistor.[30] In this model, the device noise parameters are obtained from the elements of the equivalent circuit of the transistor and two frequency independent constants, the equivalent gate temperature (T_g), and equivalent drain temperature (T_d). The equivalent circuit of the InP HEMT is shown in Fig. 2.1. All resistive elements are assigned with T_g, except the drain conductance (g_{ds}) which is assigned with T_d. It is generally accepted that T_g is approximated to the ambient temperature implying that the source of the noise is thermal. Upon cooling the device to cryogenic temperatures, the device temperature may not be the same as the ambient temperature, in particular below 30 K.[31] The intrinsic device temperature is restricted due to self-heating at low temperature thus T_g can be higher than the ambient temperature.[31]

T_d does not strongly depend on the device ambient temperature and there-

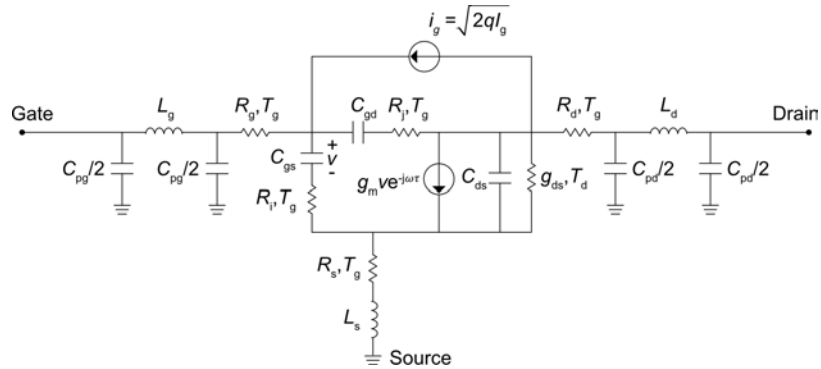


Figure 2.1: Small-signal and noise model of the InP HEMT.[11]

fore not of thermal origin.[4,28] It is known that T_d depends linearly on the drain current (I_d), and accounts for average electron temperature in a direction parallel to the channel.[12,32] In most of the channel, carriers travel at saturated velocities and therefore T_d can be interpreted as a parameter representing the hot-electron noise in the HEMT.

The noise parameters of the HEMT are the minimum noise temperature (T_{min}), the optimum source impedance ($Z_{opt} = R_{opt} + jX_{opt}$) for obtaining T_{min}, and the noise conductance (g_n):[12]

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{R_t T_g g_{ds} T_d}, \tag{2.1}$$

$$X_{opt} = \frac{1}{\omega C_{gs}}, \tag{2.2}$$

$$R_{opt} \approx \frac{f_T}{f}\sqrt{\frac{R_i T_g}{g_{ds} T_d}}, \tag{2.3}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds} T_d}{T_o}, \tag{2.4}$$

where f_T is the intrinsic cut-off frequency, R_t is the sum of R_g, R_i, R_s, where R_g is the gate resistance, R_i is the intrinsic gate-source resistance, and R_s is the source resistance, C_{gs} is the gate-source capacitance, and T_o is the standard temperature of 290 K. Eq. 2.1 indicates that a HEMT with higher f_T and lower parasitic resistances leads to a reduction in T_{min}. In Eq. 2.1, f_T and T_d are the strong bias-dependent parameters. As f_T and T_d are proportional to g_m and I_d, respectively, the optimum bias of T_{min} corresponds to the minimum value of:[12]

$$f(V_{ds}, I_d) = \frac{\sqrt{I_d}}{g_m}. \tag{2.5}$$

This implies that the low-noise HEMT must achieve a high g_m at a low value of I_d. This means that the noise level in the HEMT can be improved by scaling, i.e. smaller gate-length and thinner barrier thickness. However, this also leads to increased gate leakage current. In this case, the noise model should include the influence of the noise generated by the gate leakage current. The gate current influence of noise is treated as a pure shot noise current source:[33]

$$i_g = \sqrt{2qI_g}, \tag{2.6}$$

where I_g is the measured gate leakage current. Fig. 2.1 shows the noise model with the gate leakage current source. At the low frequency limit,[33] T_{min} can be approximated as

$$T_{min} \approx \sqrt{2qI_gR_t\frac{T_g}{k}}. \tag{2.7}$$

T_{min} is almost frequency independent with I_g, and therefore the I_g will strongly influence T_{min} at sufficiently low frequencies.[28,33] Although the value of I_g decreases at cryogenic temperatures, the relative contribution of I_g with respect to T_{min} becomes more significant since the thermal noise contributions are largely reduced.

With frequency dependent noise parameters, the low-noise amplifier can be designed in the specified frequencies. By knowing the equivalent circuit of the transistor and the two frequency independent constants T_g and T_d, the noise parameters of the transistor are obtained.

2.2 Noise modeling method

Since T_{min} of the HEMT at cryogenic temperature is very low, the device noise is extracted by an indirect method. T_{min} can be modeled by assembling the HEMT in a known LNA and performing a noise measurement of the LNA. To evaluate the noise performance of various HEMTs, the LNA design is insensitive with respect to the input matching so that variation in the LNA noise temperatures is from the device noise property. For example, in the input matching, an inductive feedback consisting of long bond wires between the source of the transistor and ground is used.[10] Such inductive feedback reduces the imaginary part of the optimum noise source impedance making the LNA design relatively insensitive to the input matching.

When the equivalent circuit parameters of the HEMT are known, the noise temperature of the HEMT LNA can be simulated provided T_g and T_d are known. Assuming T_g is the ambient temperature,[12] the only unknown parameter is T_d. T_d is obtained by fitting the simulated noise temperature of the LNA with the measurement data. In this way, T_{min} of the HEMT can be obtained.

For cryogenic low-noise InP HEMTs, it is essential to maximize f_T in the low drain current region while keeping the gate leakage current low. In the

next chapter, the epitaxial structure and device fabrication of the InP HEMT technology optimized for cryogenic low-noise performance are discussed.

Chapter 3

InP HEMT Technology

The noise properties of the InP HEMT are largely dependent upon the device technology. A key requirement for the low-noise InP HEMT technology is to optimize for a high gain and transconductance at low drain current when operating under cryogenic temperatures. Since the cryogenic LNA noise performance is to a major part dependent upon the transistor noise properties, the InP HEMT technology becomes crucial.

In this chapter, the InP HEMT technology used in this thesis for cryogenic LNA designs are presented. The technology will be discussed in terms of the epitaxial design and the fabrication process.

3.1 Epitaxial structure

The epitaxial structures investigated in this thesis are presented in Fig. 3.1. The epitaxial layers, from the top to the bottom, consist of an InGaAs cap layer, an InP etch stop layer (in *structures B* and *C*), an InAlAs barrier layer, an InGaAs channel layer, a pseudomorphic InAlAs buffer layer, and semi-insulting InP substrate. The layers were grown by molecular beam epitaxy (MBE).

The highly Si-doped InGaAs cap layer was used for source and drain ohmic contacts yielding a low value of contact resistance. A typical sheet resistance (R_{sh}) of the cap layer was about 55 $\Omega/\square$ at 300 K. R_{sh} reduced by a factor of about three when cooled down to 5 K.

Below the InGaAs cap layer, a wide bandgap InAlAs was employed as a barrier layer. The barrier composition and thickness affected the Schottky barrier height, the threshold voltage, and transconductance. In this work, the barrier composition was fixed to $In_{0.52}Al_{0.47}As$, which is lattice matched to InP, and various barrier thicknesses were investigated. By thinning down the barrier layer, the gate-to-channel distance can be reduced. The electrons are accelerated more quickly at reduced gate-to-channel distance, increasing f_T.[34] Experimental results of the influence of the barrier thickness on the cryogenic HEMT noise follow in the next chapters.

It is noted that the InP etch stop layer was included in *structures B* and *C* on top of the barrier layer in Fig. 3.1. T. Enoki *et al.* introduced the InP etch stop layer to improve the selectivity in the etching of the cap to the barrier.[35] In addition, the InP etch stop layer helped to eliminate the kink effect by passivating deep level defects on the surface of the InAlAs barrier layer.[36,37] These deep level traps are located close to the middle

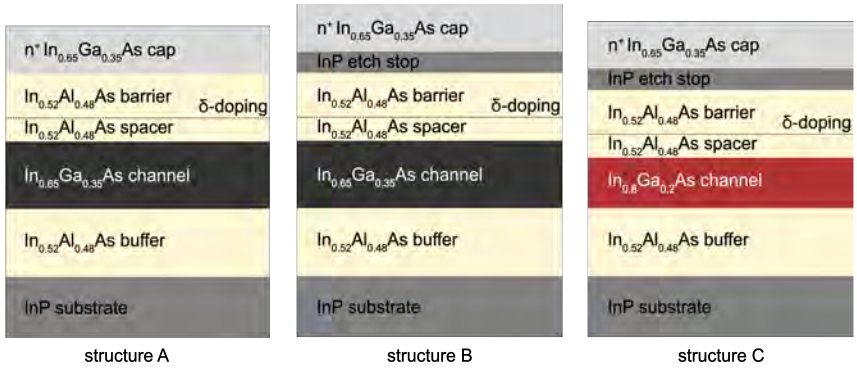


Figure 3.1: The InP HEMT epitaxial layer structures investigated in this thesis.

of the bandgap. The electron trap and release phenomenon appear as a kink in the output characteristics, which becomes more evident at cryogenic temperatures.[32,38] This is because at room temperature, the trapped electrons are released by thermal excitation, whereas at cryogenic temperatures, electron confinement improves as the thermal energy of electrons decreases, which in turn increases the influence of traps.[32,39] The kink effect increases the output conductance in the dc characteristics. Furthermore, the surface traps deplete the channel electron density under the recessed region, increasing the access resistances.[40] In the InP layer, the Fermi pinning level is close to the conduction band minimum so that sufficient electron density in the recessed region is maintained, suppressing the kink.[40,41] Thus, the InP etch stop layer can be an important structure for cryogenic operation of the InP HEMT.

The Si δ-doping supplies electrons into the InGaAs channel layer. The doping concentration was calibrated during MBE growth in order to target a specified electron sheet density (n_s). Between the wide bandgap InAlAs and a narrow bandgap InGaAs layer, electrons are confined by the two potential barriers. The motion of electrons are restricted in the plane parallel to the channel where the 2DEG is formed. Since the ionized dopants are separated from the electrons, the impurity scattering becomes suppressed resulting in high electron mobility (μ_n) in the channel. The $In_{0.65}Ga_{0.35}As$ exhibits the electron mobility of around 17 000 $cm^2/V{\cdot}s$ at 300 K.[42] Although InSb has a superior electron mobility, i.e. 77 000 $cm^2/V{\cdot}s$ at 300 K,[43] compared to InGaAs, the InSb HEMT does not exhibit low-noise performance due to high gate current and high output conductance associated with severe impact ionization.[43,44]

The electron mobility in the InGaAs channel improves with increasing indium content. This is related to the smaller effective electron mass and a narrower bandgap, resulting in a larger conduction band offset and improved carrier confinement to the channel layer. However, the lattice constant increases with indium content, increasing the lattice mismatch between the InGaAs and the InAlAs. If the InGaAs layer is thin enough, the layer can be physically

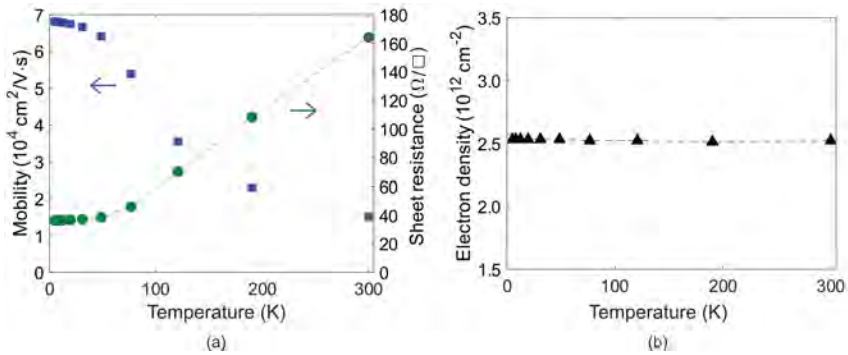


Figure 3.2: (a) Electron mobility (left) and sheet resistance (right) and (b) electron sheet density in the channel as a function of the temperature. The measurements were done in *structure C*. Courtesy of Junjie Li.

strained so that the lattice constant becomes the same as the InAlAs, and dislocations can be avoided. The critical thickness (t_c) can be estimated by the empirical formula $t_c \approx a_e^2/(2|a_e - a_s|)$, where a_e and a_s are the lattice constants of the epitaxial layer and substrate, respectively.[45] Taking the lattice constant of InGaAs to a_e and InAlAs to a_s, the critical thickness for $In_{0.65}Ga_{0.35}As$ and $In_{0.8}Ga_{0.2}As$ is about 35 nm and 16 nm, respectively. In this work, the thickness of each layer was about half the critical thickness so the strain generated due to lattice mismatch was absorbed entirely by the lattice.

The Hall bar measurements of *structure C* without the cap layer are shown in Fig. 3.2. The measurements were done from 300 K down to 5 K. μ_n of 15 000 cm^2/V·s was measured at 300 K, and improved to 70 000 cm^2/V·s when cooled down. R_{sh} of the channel layer was 160 Ω/□ at 300 K, and reduced to 40 Ω/□ when cooled down to 5 K. n_s remained constant around 2.5 $\times 10^{12}$cm^{-2}. Below the channel layer, a 500 nm thick pseudomorphic InAlAs buffer layers was grown on the InP substrate.

3.2 Device fabrication

The most critical parts of the InP HEMT fabrication is to achieve a low access resistance, a selective gate recess etching, and a T-gate process. Fig. 3.3 shows the process flow of the device fabrication used in this thesis. The key details of the device fabrication were the following:

(a) **Mesa etching** - Electrically isolation of the device from other devices was done by wet etching of the InGaAs and InAlAs layers using a H_2O_2:H_3PO_4:H_2O (1:1:25) solution, and of the InP layer using a HCl:H_2O (1.5:1) solution.

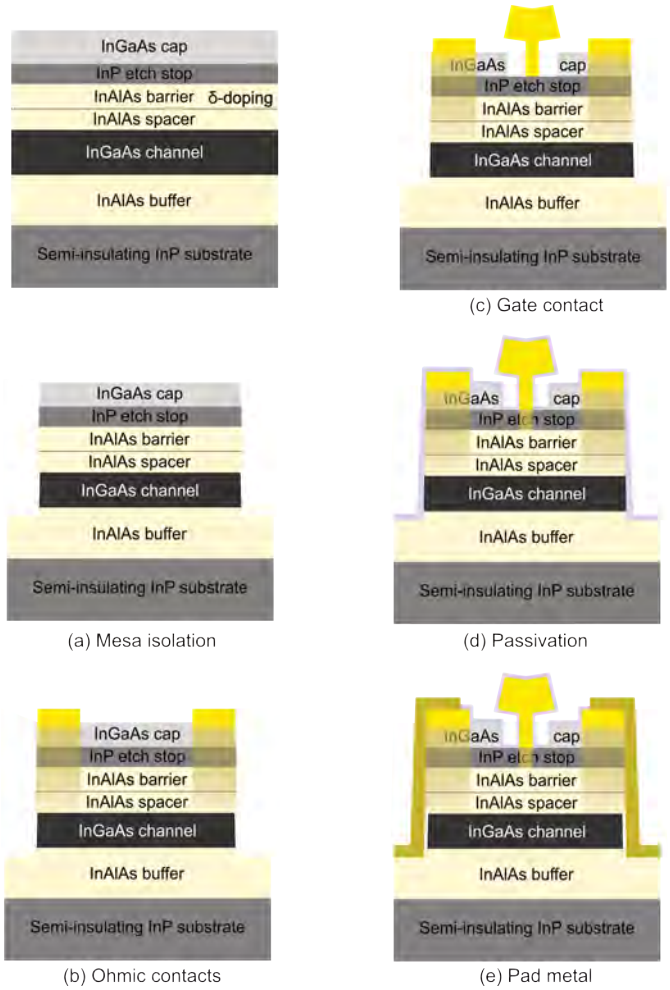


Figure 3.3: Schematic of fabrication processes for the InP HEMT.

(b) **Source and drain contact formation** - The source and drain ohmic contacts were formed with alloyed NiGeAu. The contact resistance was optimized by adjusting the annealing temperature and duration in the rapid thermal annealer.[46] The contact resistance was measured using the transmission line method. A typical contact resistance was about 0.03 Ω·mm at 300 K. The distance between the source and the drain contact was 1.4 μm.[46]

(c) **Gate contact formation** - The T-shaped gate contact was defined by electron beam lithography. Prior to the gate metal deposition, the InGaAs cap layer was wet etched, known as the gate recess etching

process. The cap layer must be removed for a Schottky gate contact with low reverse current. Since the depth and width of the recess etching strongly affect the device performance, such as the gate leakage current, transconductance, access resistances, and threshold voltage, it is important that the recess etching is highly selective. The gate recess etching was performed using a succinic acid/H_2O_2 (4.5:1) solution (for *structure A* in Fig. 3.1(a)) or a citric acid/H_2O_2 (7:1) solution (for *structures B* and *C* in Fig. 3.1(b) and (c)). The succinic acid based wet etchant is commonly used for etching the InGaAs selectively against the InAlAs. The selectivity of the InGaAs cap recess etch to the InAlAs barrier using the succinic acid is greater than 70:1.[47] On the other hand, the citric acid used for etching the InGaAs against the InP has a selectivity greater than 400:1.[48]

The gate metal stack of Ti/Pt/Au or Pt/Ti/Pt/Au was deposited by electron beam evaporation. The Ti is a conventional gate metal on the InAlAs barrier layer with a Schottky barrier height of 0.65 eV,[49] whereas the Pt gate on the InAlAs offers a higher Schottky barrier height than the Ti gate (i.e. 0.83 eV[50]) which can suppress the gate leakage current.[51–54] The influence of the gate metal on the gate leakage current will be presented in Chapter 4.

(d) **Passivation** - After the lift-off of the gate metal stack, the device was passivated either with Si_3N_4 using plasma-enhanced chemical vapor deposition at 270 °C or Al_2O_3 using atomic layer deposition (ALD) at 250 °C. For the Pt gate, 250 °C was enough to make Pt gate metal diffuse through the InP etch stop layer in the case of *structures B* and *C*.[50] The passivation was thus often done with ALD for the Pt gate metal.

(e) **Pad metallization** - After removing the passivation (Si_3N_4 by reactive ion etching or Al_2O_3 by HF:H_2O), the Ti/Au metal stack for probing pads was deposited by electron beam evaporation.

The optimization of InP HEMT technology for cryogenic LNAs in this thesis was mainly focused on the design of the barrier layer and the channel structure, the selective gate recess etching, and gate metal formation. The impact on the InP HEMT performance and cryogenic noise properties are presented in the next Chapters 4 and 5.

Chapter 4

Scaling of the InP HEMT for Cryogenic LNAs

According to the noise model of the InP HEMT described in Chapter 2, low-noise properties can be improved by enhancing f_T from device scaling. However, device scaling tends to increase the gate leakage current which is detrimental to the noise properties at low frequencies (i.e. at few GHz range).[3,12,17,18] Further research on the trade-off between scaling of the HEMT and the gate leakage current is necessary for advances in the noise performance at cryogenic temperatures. As the gate leakage current is process and epitaxial structure dependent, it is necessary to evaluate the impact of the gate current experimentally on a specific HEMT process.

This chapter addresses the characterization of the scaled InP HEMTs in terms of dc and rf performance. The influence of the gate leakage current on the noise performance of HEMTs and cryogenic LNAs up to 30 GHz is discussed.

4.1 InP HEMT characterization

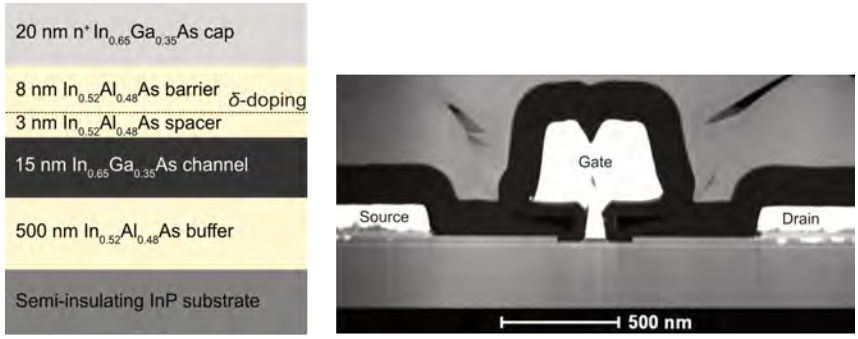
The expression for f_T is given as[55]

$$f_T = \frac{g_{m,i}}{2\pi} \frac{1}{(C_{gs}+C_{gd}) + g_{m,i}C_{gd}(R_s+R_d)[1+(1+\frac{C_{gs}}{C_{gd}})\frac{g_{ds}}{g_{m,i}}]} \tag{4.1}$$

where $g_{m,i}$ is the intrinsic transconductance, C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, R_s and R_d are the source and drain resistances, and g_{ds} is the drain conductance.

In order to improve f_T, $g_{m,i}$ should be as high as possible. In order to achieve that, the gate should then be located close to the channel. However, this will lead to an increase of C_{gs} and C_{gd}. Since C_{gs} and C_{gd} are linearly dependent upon the gate-length (L_g), scaling of L_g as well as the gate-to-channel distance will lead to an improvement in f_T.

In a previous work, a 130 nm gate-length InP HEMT technology with an 11 nm thick barrier was used for demonstrating a 0.5−13 GHz MMIC LNA at cryogenic operation.[11] In this thesis, the experiment was repeated in the same process using a 100 nm gate-length and an 8 nm barrier thickness. A thinner barrier implies that the I_g was expected to increase and thus act



(a) (b)

Figure 4.1: (a) The epitaxial layer structure of the InP HEMT with 8 nm barrier layer thickness. (b) STEM image of the 100 nm gate-length HEMT in the gate region, showing the gate (Ti/Pt/Au metal stack) and ohmic contacts as well.

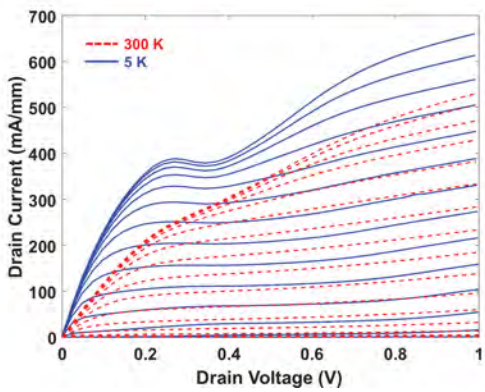


Figure 4.2: Output characteristics of a 2 × 100 μm gate width and 100 nm gate-length InP HEMT. V_{gs} measured from −0.5 V to 0.4 V in steps of 0.04 V (Paper [B]).

detrimentally to the noise properties of the cryogenic LNA. On the other hand, the scaling itself would increase g_m and f_T thus improving noise. By comparing these two structures, the influence of scaling on cryogenic noise was studied. The epitaxial layer structure used in this study is shown in Fig. 4.1(a), corresponding to *structure A* in Fig. 3.1. μ_n and n_s were 10 850 cm^2/V·s and 3.3 × 10^{12} cm^{-2} at 300 K, respectively. A cross-sectional STEM image in Fig. 4.1(b) shows the InP HEMT processed as described in Chapter 3. The gate-length was 100 nm and a Ti/Pt/Au gate metal stack was used.

Fig. 4.2 shows the output characteristics of a 2×100 μm HEMT. The maximum drain current density at a drain-source voltage (V_{ds}) of 1 V was

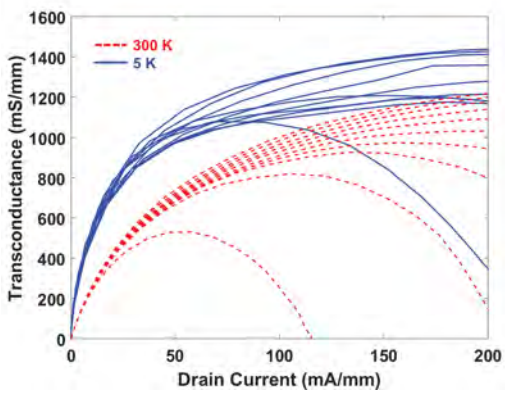


Figure 4.3: Extrinsic dc g_m versus I_d. V_{ds} measured from 0.1 V to 1 V in steps of 0.1 V (Paper [B]).

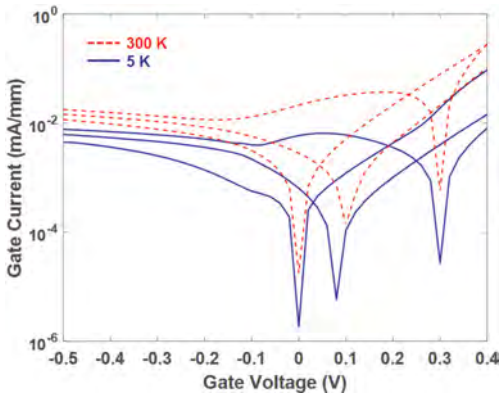


Figure 4.4: Gate current of the InP HEMT at 300 K and 5 K. V_{ds} measured from 0 V to 1 V in steps of 0.5 V (Paper [B]).

500 mA/mm at 300 K and 650 mA/mm at 5 K. A kink in the drain current for about $V_{ds} = 0.3$ V was observed at 5 K. This is known to be related to the traps at the epitaxial interfaces, the buffer layer, and surface in the gate recess region.[36,38,56,57] Although the kink in Fig. 4.2 close to the pinch-off region was not obvious, the presence of traps can cause low frequency dispersion in g_m, and a change in the channel electron density.[40,56] Hence a device with a suppressed kink is desirable, in particular at cryogenic temperatures.

The dc extrinsic g_m as a function of I_d is shown in Fig. 4.3. The slope of g_m at very low I_d is an important indicator of the low-noise performance of the HEMT during the dc characterization as seen in Eq. 2.5.[12] At 5 K, g_m reached 1 S/mm at I_d of only 40 mA/mm at $V_{ds} = 1$ V. The device with a scaled barrier layer exhibited a steeper increase of g_m compared with the

Table 4.1: Small-signal modeling parameters of 2×100 μm InP HEMT at the optimum low-noise bias at 5 K. Units are V, mA, μA/mm, fF, mS, and Ω.

		L_g = 100 nm d_B = 8 nm	L_g = 130 nm d_B = 11 nm
Bias	V_{ds}	0.4	0.6
	I_d	5	5
	I_g	1.2	0.45
Intrinsic	C_{gs}	139	148
	C_{gd}	43	36
	C_{ds}	59	51
	$g_{m,i}$	244	223
	g_{ds}	17	14
Extrinsic	R_g	0.6	2
	R_d	0.8	2
	R_s	0.8	1

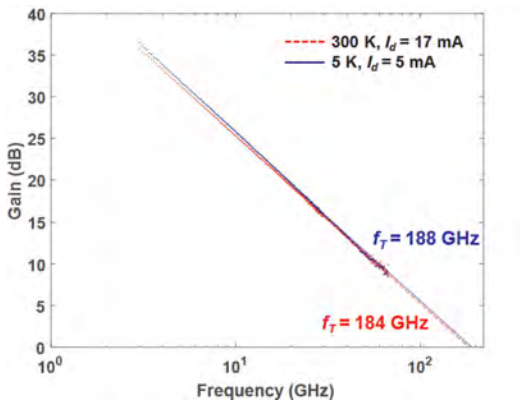


Figure 4.5: Intrinsic current gain $|H_{21}|^2$ of the InP HEMT at the optimum low-noise bias at 300 K (red dashed) and 5 K (blue solid) (Paper [B]).

device with a thicker barrier,[32] where a g_m of 1 S/mm was obtained for I_d of 50 mA/mm.

Fig. 4.4 shows the gate leakage current versus the gate-source voltage (V_{gs}) at 300 K and 5 K. The noise-optimized bias condition at 5 K was V_{ds} = 0.4 V and I_d = 5 mA where the measured I_g was in the order of 1 μA/mm which was a factor of three higher compared to the thicker barrier HEMT.[11]

The S-parameter measurements were carried out up to 67 GHz at 300 K and 5 K. The system was calibrated with a GGB CS-5 alumina substrate using through-reflect-match calibration. Equivalent circuit parameters at the optimum low-noise bias conditions were obtained using a direct extraction method.[58,59] A comparison of the small-signal modeling parameters between

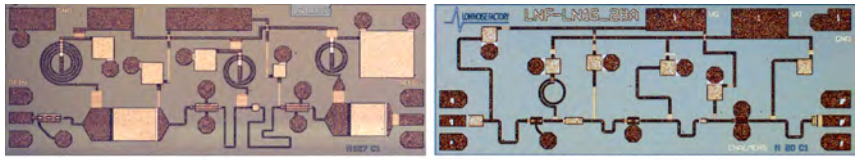


Figure 4.6: MMIC photographs of (a) the 0.3–14 GHz HEMT LNA and (b) the 16–28 GHz HEMT LNA. Both chip sizes were 2 mm × 0.75 mm (Paper [B]).

the two HEMTs with different L_g and d_B is presented in Table 4.1. The scaled device improved $g_{m,i}$ about 10% at 5 K whereas the total gate capacitances were comparable. Fig. 4.5 shows the intrinsic current gain $|H_{21}|^2$ of the scaled InP HEMT. The extrapolated f_T with a slope of – 20 dB/dec was 188 GHz at 5 K. This corresponded to a 10% increase in f_T.[32] In the next section, the two LNAs operating up to 30 GHz based on the presented InP HEMT technology are demonstrated, and the InP HEMT noise properties at cryogenic temperatures are discussed.

4.2 InP HEMT noise properties

The low-noise InP HEMTs with $L_g = 100$ nm and $d_B = 8$ nm were implemented in 0.3−14 GHz and 16−28 GHz MMIC LNAs. Fig. 4.6 shows photographs of the fabricated MMIC chips. The three-stage 0.3−14 GHz LNA used 2 × 100 μm HEMTs and the 16−28 GHz LNA 2 × 50 μm HEMTs. For further details on the MMIC design and the LNA performance at room temperature, see Paper [B].

At an ambient temperature of 4 K, the optimum low-noise bias for the 0.3−14 GHz LNA was $V_D = 0.8$ V and $I_D = 15$ mA. Fig. 4.7 presents the noise temperature (T_e) and gain of the LNA. The amplifier achieved an average noise temperature ($T_{e,avg}$) of 3.5 K and a 41.6 dB gain. The 16−28 GHz LNA was biased for lowest noise at $V_D = 0.5$ V and $I_D = 7$ mA and achieved $T_{e,avg}$ of 6.3 K and 32.3 dB gain, as shown in Fig. 4.8. For comparable wide bandwidth designs, the two cryogenic LNAs both exhibited state-of-the-art results in terms of the lowest noise temperature and highest gain per stage[2,4,11,60–63] (Paper [B]).

The improved noise result for the 0.3−14 GHz MMIC LNA in this thesis compared to the previous work[11] was obtained by device scaling. This means an inevitable increase in I_g for the InP HEMT which is well-known to counteract the noise improvement.[3,12,17,18] The effect of I_g on cryogenic T_e of the LNA and T_{min} of the HEMT was simulated with different values of I_g in Figs. 4.9 and 4.10. It was observed that the impact of I_g on T_{min} is much stronger at low frequencies.[3,12,17,18] While the increased I_g significantly deteriorated T_{min} at low frequencies, I_g affected the LNA noise temperature less. This

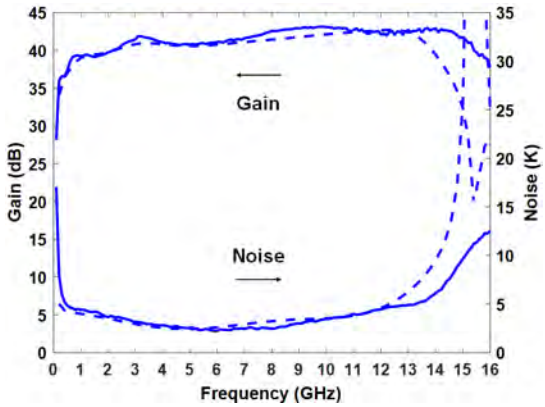


Figure 4.7: Measured (solid line) and simulated (dashed line) gain and noise temperature of the 0.3–14 GHz LNA at 4 K. The optimum noise bias for the LNA was $V_D = 0.8$ V, $I_D = 15$ mA (Paper [B]).

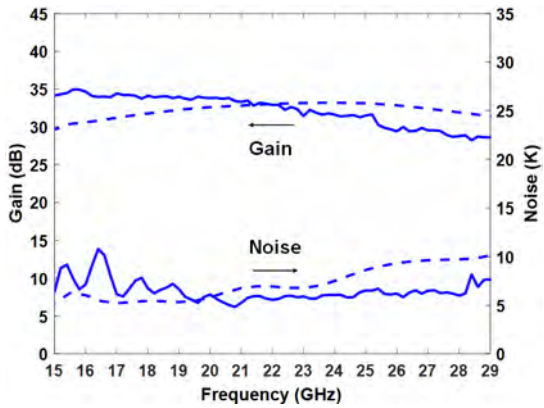


Figure 4.8: Measured (solid line) and simulated (dashed line) gain and noise temperature of the 16–28 GHz LNA at 4 K. The optimum noise bias for the LNA was $V_D = 0.5$ V, $I_D = 7$ mA (Paper [B]).

was because the transistor was mismatched for noise at low frequencies, but very well matched at high frequencies. The I_g of 1.2 μA/mm made a small difference increasing the noise temperature of the LNA by about + 6% at 6 GHz compared to that without I_g. The presented I_g was still small enough to not dominate the cryogenic noise performance. Thus it is interpreted that the improved f_T brought an overall improvement in cryogenic InP HEMT LNA noise performance.

In Fig. 4.9, it was predicted that a further increase in I_g degraded the noise performance significantly in the frequency range below 10 GHz. On the other hand, this effect was much less severe at high frequencies as plotted

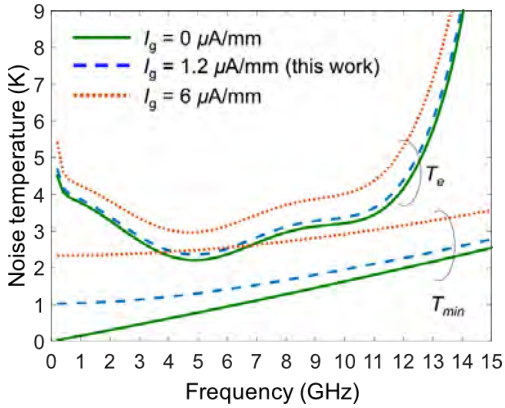


Figure 4.9: The simulated T_e of the LNA and T_{min} of the HEMT with 1.2 μA/mm gate current (dashed) at 10 K compared with the same device without gate current (solid) and with 6 μA/mm gate current (dotted) at 0.3–14 GHz (Paper [B]).

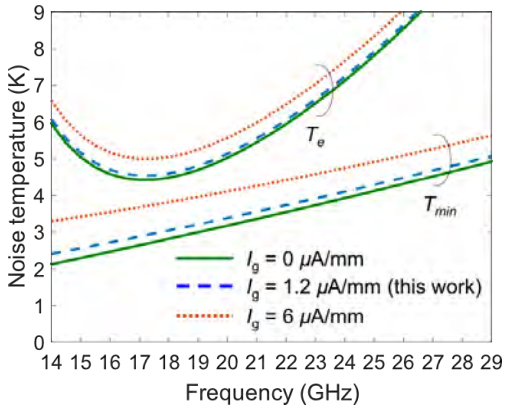


Figure 4.10: The simulated T_e of the LNA and T_{min} of the HEMT with 1.2 μA/mm gate current (dashed) at 10 K compared with the same device without gate current (solid) and with 6 μA/mm gate current (dotted) at 16–28 GHz (Paper [B]).

in Fig. 4.10. Further noise improvement via scaling can only be determined experimentally and might only be valid for a specific process since the gate current is process dependent. This study indicated that the HEMT process based on the epitaxial design of *structure A* in Fig. 3.1 was close to the limit in T_{min} in the frequency range below 10 GHz since the noise was predicted to be dominated by a higher gate leakage current as shown in Fig. 4.9.

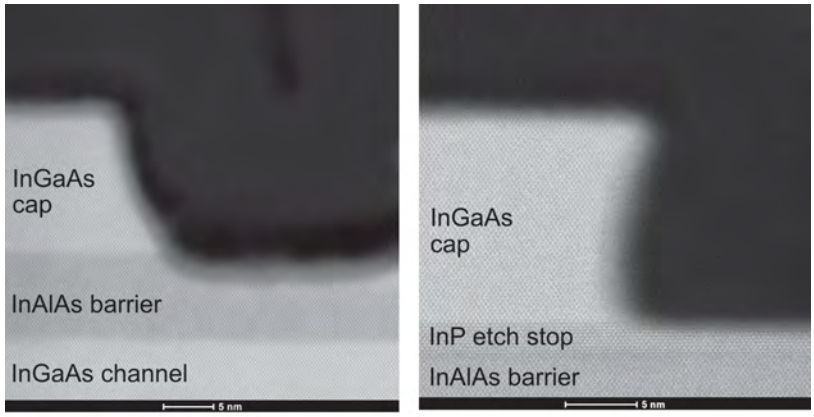


Figure 4.11: STEM images focused on the gate recess region of the epitaxial layers (a) without the InP etch stop layer (*structure A*) and (b) with the InP etch stop layer (*structures B* and *C*).

4.3 InP HEMT with InP etch stop layer

In section 4.2, it was demonstrated that the increased I_g counteracted improvements in T_{min} of the transistor, in particular below 10 GHz. This suggests that further scaling of the barrier must be performed without compromising I_g. The gate leakage current largely depends on gate recess etching and gate metal formation. The STEM image in Fig. 4.11(a) presents the gate recess region of *structure A* in Fig. 3.1. It clearly shows the over-etched barrier layer in *structure A*. In addition, the etching was non-uniform in the recess region. This will lead to a process variation from device to device, thus less control over I_g. It was concluded that a new epitaxial design was needed in the InP HEMT gate process allowing a more selective recess etching.

In this work, an InP etch stop layer was inserted on top of the InAlAs barrier layer. It is well-known that the InP etch stop layer inserted between the InGaAs cap and InAlAs barrier layers (*structures B* and *C* in Fig. 3.1) has proven to improve the recess etching.[35,36,54] As seen in Fig. 4.11(b), the InP HEMT with the etch stop layer exhibited a flat and sharp gate recess.

Another advantage of the InP etch stop layer is to eliminate the kink effect in the InP HEMT output current.[36,37] An oxidation ratio between the InP and InAlAs of 1:80 was reported.[64] While the Fermi level pinning is reported to be 0.1 eV below the conduction band minimum in the InP,[65] the Fermi level pinning in the InAlAs is about 0.6 eV.[66] This explains the pronounced kink phenomena observed in the HEMT with the InAlAs barrier layer.[32,38] The HEMTs with an InP etch stop layer have been reported to strongly suppress the kink effect at room temperature.[36,54,67] As the barrier layer is scaled, bringing the channel closer to the surface, the influence of the surface trap

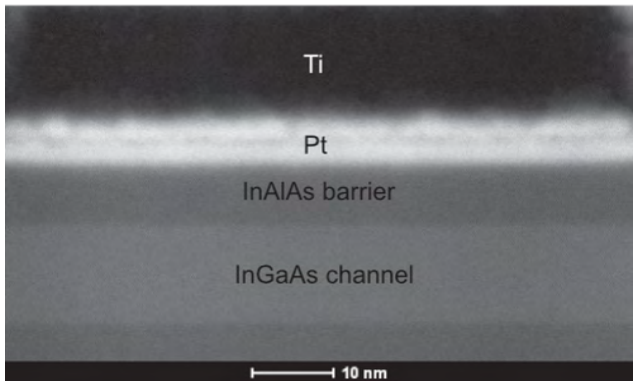


Figure 4.12: STEM images of the the HEMT with a 3 nm InP etch stop, a 8 nm InAlAs barrier, a 3 nm InAlAs spacer, and 15 nm InGaAs channel layers. The Pt gate metal formed a Schottky contact to the InAlAs layer.

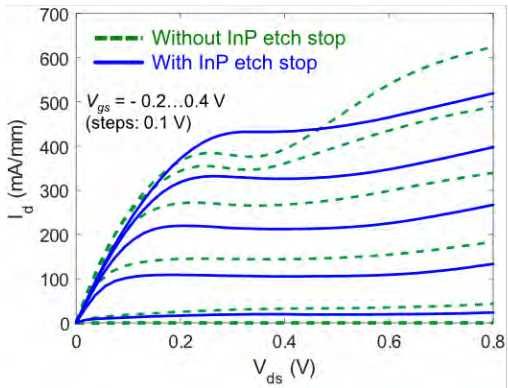


Figure 4.13: I_d versus V_{ds} of the InP HEMT without and with the InP etch stop layer at 5 K. Both InP HEMTs had d_B of 8 nm.

will be more severe. In this thesis, this effect is also verified for cryogenic temperature operation of the InP HEMT.

A gate metal with a high Schottky barrier height contributes to a reduction of I_g. As mentioned in Chapter 3, the Pt gate on the InAlAs has a higher Schottky barriers of 0.83 eV[50] than the Ti (0.65 eV)[49] which can prevent excessive gate leakage.[51–54] Experiments by K. Shinohara *et al.* successfully demonstrated that Pt can be sunk in through an InP etch stop layer and into an underlying InAlAs barrier by annealing at 250 °C.[51] The Pt diffusion depth can be controlled varying the Pt thickness and annealing conditions.[51–53] In this work, the 3 nm Pt gate metal was diffused during the deposition of passivation layer at 250 °C. In Fig. 4.12, a uniformly diffused Pt to the InAlAs layer is confirmed.

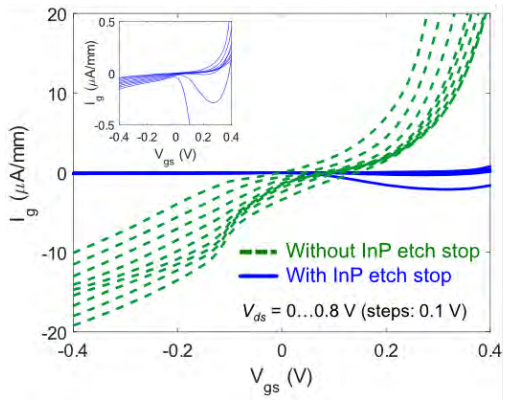


Figure 4.14: I_g versus V_{gs} at 5 K. The inset shows I_g of the InP etch stop layer with a different scale of y-axis.

Fig. 4.13 compares the dc characteristics of InP HEMTs with and without the InP etch stop layer measured at 5 K. The two devices had the same d_B. The two HEMTs exhibited a clear difference in the output characteristics. With the InP etch stop layer, the kink was effectively suppressed. Note that the maximum I_d was lower in the device using the InP etch stop layer. This was due to different gate-to-channel distance for the two structures.

The reduction in I_g at 5 K using an InP etch stop layer is shown in Fig. 4.14. The HEMT with the etch stop layer exhibited a reverse I_g at $V_{ds} =$ 0 V of about 20 nA/mm which was a factor of 500 lower than the HEMT without the etch stop layer. This means that introducing an InP etch stop layer is beneficial for further scaling of the barrier layer for low-noise cryogenic HEMTs, in particular at low frequency designs. The next chapter presents the noise performance of scaled HEMTs in the presence of the InP etch stop layer.

4.4 Summary

The InP HEMT technology with the scaled barrier thickness and gate length have been characterized in terms of dc, rf, and noise performance up to 30 GHz at cryogenic temperature. The scaling improved $g_{m,i}$ and f_T, but increased I_g as well. However, I_g was sufficiently low to not dominate the noise, so the improved f_T resulted in an overall improvement in 0.3–14 GHz cryogenic MMIC LNA noise performance. It was predicted that a further increase in I_g degraded the noise performance significantly in the frequency range below 10 GHz. This study indicated that the HEMT process based on the epitaxial design of *structure A* in Fig. 3.1 was close to the limit in T_{min} since the noise was predicted to be dominated by a higher gate leakage current. In order to perform further scaling of the barrier without compromising I_g, the

heterostructure with an InP etch stop layer inserted on top of the InAlAs barrier layer was studied. A HEMT structure using an InP etch stop layer combined with Pt gate metal showed remarkable decrease in the gate leakage current which opens up the possibility of further scaling for cryogenic LNAs.

Chapter 5

InP HEMT Optimization for Cryogenic Low-Power LNAs

In a recent demonstration of a 54 qubit quantum processor, cryogenic 4–8 GHz (C−band) InP HEMT LNAs were implemented at the 4 K stage for qubit readout.[19] One cryogenic LNA was required for every 5−10 qubits, and the dc power dissipation (P_{dc}) of the HEMT LNA was about 5 mW.[3,19,68] In order to scale up quantum computers to the millions of qubit level, the dc power must be reduced considering the potential integration of thousands of LNAs at the 4 K stage. In 2003, an InP HEMT C−band LNA was reported with an average noise temperature of 7.2 K with 17 dB gain at a dc power dissipation of 100 μW.[10] Since then, effort to optimize the noise properties of InP HEMTs for ultra-low power LNAs has been limited.

In this chapter, the feasibility of low-noise HEMT technology for ultra-low power cryogenic LNAs is investigated. It is demonstrated that low-power cryogenic InP HEMT LNAs with average noise temperature below 3 K can be realized for C−band. The effect from indium content in the InP HEMT channel has been studied in detail.

5.1 Design of low-power InP HEMT for cryogenic C−band LNAs

The optimization of low-noise HEMTs for ultra-low power requires that the device must exhibit a high g_m and f_T at very low V_{ds} and I_d. At the same time, I_g must be kept sufficiently low (i.e. $I_g < 1$ μA/mm) considering the operating frequency range in this study. One way to achieve this is a reduction of the gate-to-channel distance. However, this means that the I_g level is at a risk of being too high. In Chapter 4, the heterostructure with the InP etch stop layer effectively suppressed I_g, so further barrier scaling using this structure (*structure B* in Fig. 3.1) was selected for low-power optimization of the InP HEMT in this thesis work. The thickness of the barrier layer was scaled down to 4 nm. The previous state-of-the-art low-noise HEMTs in the 4−8 GHz range had an aspect ratio (i.e. gate-length over gate-to-channel distance) of about 10,[3] while the 100 nm gate-length HEMT with the 4 nm barrier increased the aspect ratio to 20. Fig. 5.1 shows a STEM image of the HEMT showing the epitaxial layers in the gate recess region. This structure

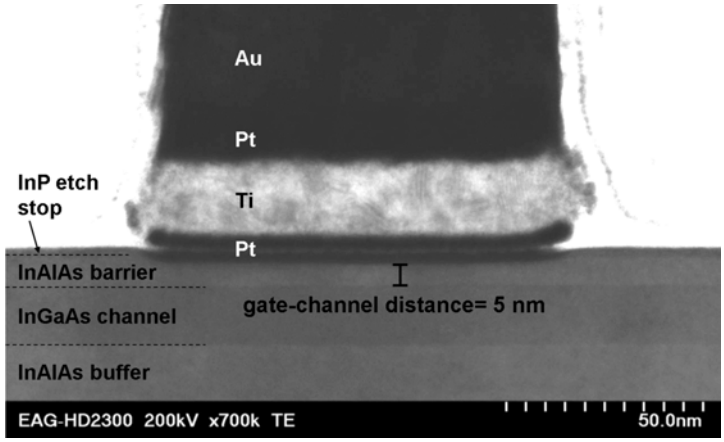


Figure 5.1: Cross-sectional STEM image of the gate region in the InP HEMT (Paper [D]).

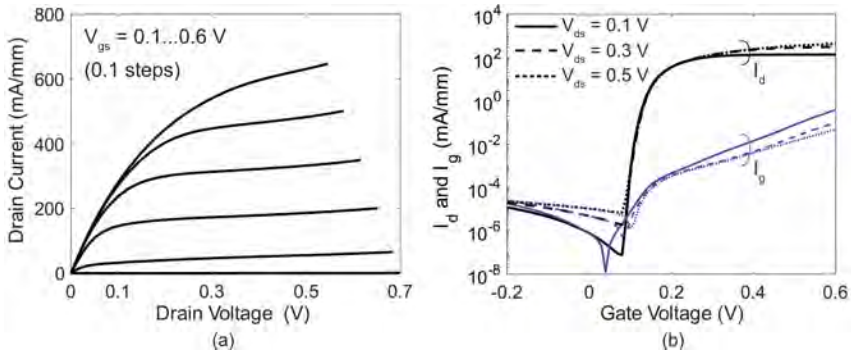


Figure 5.2: (a) I_d versus V_{ds} and (b) I_d and I_g versus V_{gs} at $V_{ds} = 0.1$ V (solid), 0.3 V (dashed), and 0.5 V (dotted). The InP HEMT with $L_g = 100$ nm and $W_g = 4 \times 50$ μm was used. The measurements were done at 5 K (Paper [D]).

consisted of a 4 nm InP etch stop layer, a 4 nm barrier layer, and a 3 nm spacer layer. A gate-to-channel distance of 5 nm was measured in Fig. 5.1. An indium (In) channel content of 65% ($In_{0.65}Ga_{0.35}As$) was used in this study.

5.1.1 HEMT characteristics

The dc characteristics at 5 K are shown in Figs. 5.2 and 5.3. In Fig. 5.2(a), the InP HEMT showed a maximum drain current of 650 mA/mm with an on-resistance of 0.32 Ω·mm at $V_{gs} = 0.6$ V at 5 K. Fig. 5.2(b) also shows SS = 14 mV/dec at $V_{ds} = 0.1$ V which is close to the lowest values experimentally observed in field-effect transistors at low temperatures ($SS \cong 11$ mV/dec

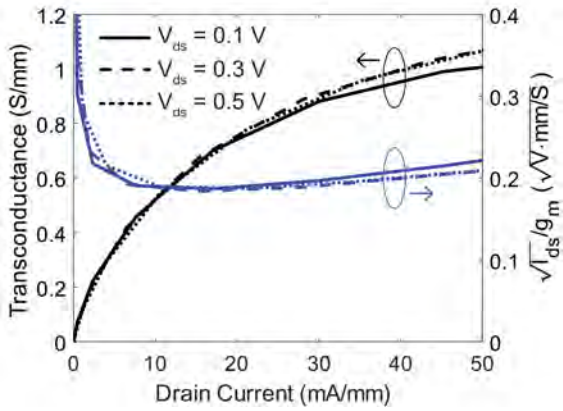


Figure 5.3: g_m and $\sqrt{I_d}/g_m$ as a function of I_d at V_{ds} = 0.1 V (solid), 0.3 V (dashed), and 0.5 V (dotted). The InP HEMT with L_g = 100 nm and W_g = 4 × 50 μm was used. The measurements were done at 5 K (Paper [D]).

at 4.2 K[69]). When the device is in the weak inversion condition, meaning close to the subthreshold region, g_m to I_d ratio depends on SS ($g_m/I_d = ln10/SS$).[45,70,71] With such a low SS, the HEMT can achieve a high g_m/I_d at low bias conditions. Fig. 5.3 shows g_m and $\sqrt{I_d}/g_m$ versus I_d at different V_{ds}. A g_m of 1 S/mm was achieved for an I_d of 40 mA/mm. Also, $\sqrt{I_d}/g_m$ exhibited its minimum value below 0.2 $\sqrt{V \cdot mm/S}$ at I_d of around 10 mA/mm. g_m as well as $\sqrt{I_d}/g_m$ did not show a strong dependence on V_{ds}, which implies that the device is promising for low-noise performance under low-power operation. I_g in Fig. 5.2(b) exhibited about 0.1 μA/mm at the low-noise region which is close to pinch-off (i.e. $V_{gs} \sim$ 0.15 V). The influence of I_g to the C−band LNA noise performance will be negligible (Paper [B]).

5.1.2 HEMT noise properties

The noise performance at cryogenic temperature for the InP HEMT with d_B of 4 nm was evaluated using a 4–8 GHz three-stage hybrid LNA.[10] Each stage was equipped with a 4 × 50 μm gate-width (W_g) transistor.

Fig. 5.4 shows the measured noise temperature and gain of the LNA at different P_{dc} at 5 K. At P_{dc} = 300 μW (V_d = 0.1 V, I_d = 3 mA), a $T_{e,min}$ of 2.4 K at 4.4 GHz with $T_{e,avg}$ of 2.8 K was achieved. The gain was 26.9 dB. When the LNA was biased for an even lower P_{dc} of 112 μW (V_d = 0.07 V, I_d = 1.6 mA), the LNA exhibited a $T_{e,min}$ of 3.2 K at 4.4 GHz with $T_{e,avg}$ of 4.1 K and a gain of 20 dB.

Fig. 5.5 shows a comparison of gain and noise between LNAs using InP HEMTs with d_B = 4 nm and 6 nm at P_{dc} = 300 μW. Both devices had the same In channel content of 65% (*structure B* in Fig. 3.1), and the same W_g. The noise performance of the InP HEMT with d_B = 6 nm at various P_{dc} can

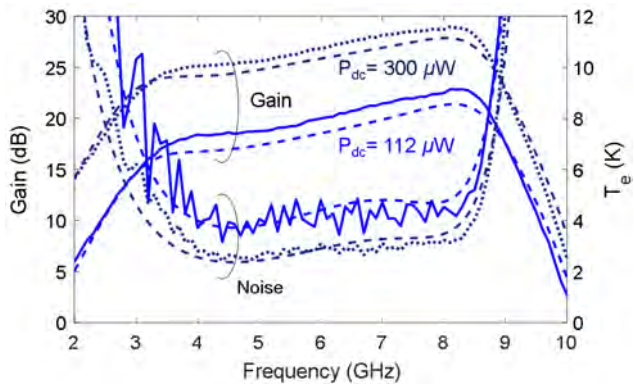


Figure 5.4: (a) Noise temperature and gain of three-stage 4–8 GHz hybrid LNAs at 5 K at different dc power dissipation. The InP HEMT with d_B of 4 nm and 65% In channel content was employed in the LNA. The amplifier was biased at $V_d = 0.1$ V, $I_d = 3$ mA ($P_{dc} = 300$ μW, dotted), and $V_d = 0.07$ V, $I_d = 1.6$ mA ($P_{dc} = 112$ μW, solid). The simulated noise temperature and gain (dashed) are also shown (Paper [D]).

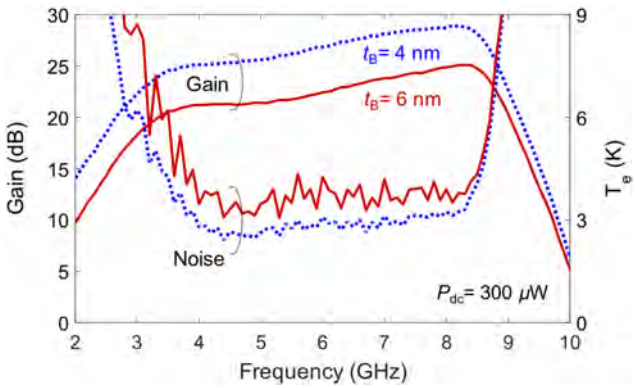


Figure 5.5: (a) Comparison of noise temperature and gain of the LNAs equipped with InP HEMTs with $d_B = 4$ nm (dotted) and $d_B = 6$ nm (solid) biased at $P_{dc} = 300$ μW at 5 K. Both HEMTs had 65% In channel content.

be found in Paper [C]. The $T_{e,avg}$ for the 4 nm barrier HEMT showed a 30% lower noise temperature with a 3 dB higher average gain at $P_{dc} = 300$ μW.

A comparison of intrinsic small-signal modelling parameters at the low-noise bias conditions between the device with $d_B = 4$ nm and 6 nm are presented in Table. 5.1. The HEMT with $d_B = 4$ nm showed an improved $g_{m,i}$ compared to the device with $d_B = 6$ nm, which resulted in an improved noise temperature.

Fig. 5.6 shows $T_{e,avg}$ versus P_{dc} for the presented LNA, together with previously published state-of-the art cryogenic noise results, working in a

Table 5.1: Intrinsic small-signal modeling parameters of the InP HEMT with different barrier thicknesses. The P_{dc} of the LNA was 300 μW at 5 K.

d_B	*Bias*	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	$g_{m,i}$ (mS)	g_{ds} (mS)
4 nm	$V_{ds} = 0.05$ V $I_d = 1$ mA	107	60	51	82	12
6 nm	$V_{ds} = 0.08$ V $I_d = 0.08$ mA	98	59	49	63	11

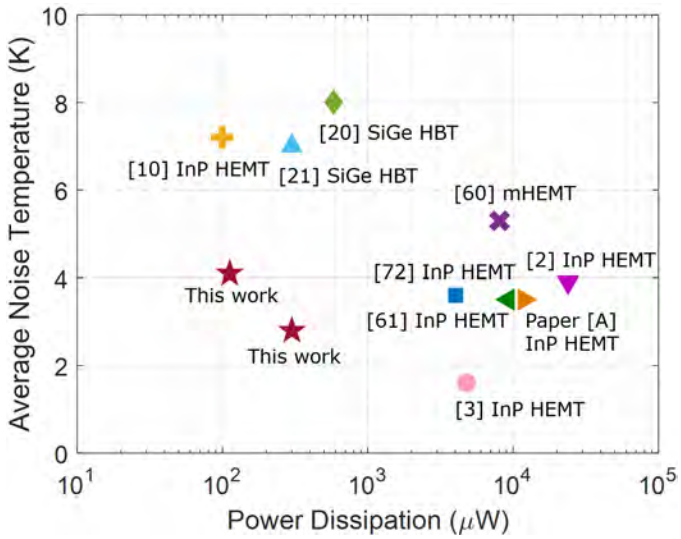


Figure 5.6: Comparison of the average noise temperature of LNAs with prior state-of-the-art results operating in C–band at cryogenic temperatures.

similar frequency range.[2,3,10,20,21,60,61,72] The work presented here resulted in excellent noise performance with a significantly lower $T_{e,avg}$ at comparable P_{dc} than prior work. The progress in power optimization presented in this thesis is attributed to the improved $g_{m,i}$ at low bias conditions by using a very short gate-to-channel distance with respect to the 100 nm gate-length device coupled with minimized gate leakage current.

5.2 Investigation of InP HEMT indium channel content

For low-power operation in which the device is biased at low V_{ds}, the low-field electron mobility becomes a more important parameter since g_m is proportional to the mobility. Thus, in principle, a channel with higher electron mobility is

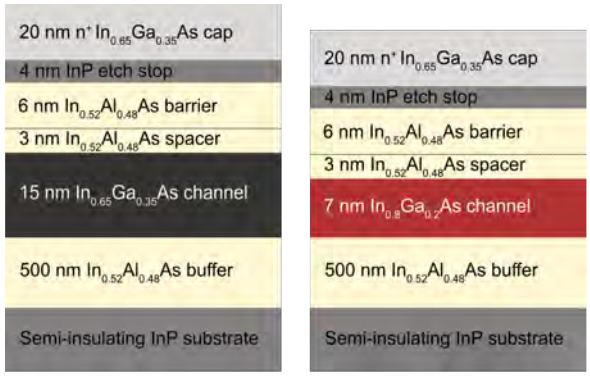


Figure 5.7: The epitaxial layer structures with two different indium channel contents (correspond to *structures B* and *C* in Fig. 3.1).

beneficial for the low-noise and high-frequency performance. The devices with enhanced mobility channel with higher indium channel contents improved the noise performance.[73, 74] However, since these investigations were focused on room temperature performance, there is a need for further research on the impact of channel structure at cryogenic temperatures.

Fig. 5.7 shows the schematic of two epitaxial InP HEMT structures with different channels, one 15 nm thick with 65% In channel, the other 7 nm thick with 80% In channel. All other layers were identical for both structures. μ_n for the 65% In and 80% In channel structures at 300 K was 12 000 and 15 000 cm^2/V·s, respectively. R_{sh} for the 65% In and 80% In channel at 300 K was 220 Ω/□ and 170 Ω/□, respectively. n_s was about 2.5 $\times 10^{12}$ cm^2/V·s in both structures.

5.2.1 HEMT characterization

Fig. 5.8 shows the dc characteristics of InP HEMTs with two different In channel contents at 300 K. In Fig. 5.8(a), the 80% In channel HEMT exhibited a reduced R_{on} from 0.46 Ω·mm to 0.44 Ω·mm, and an increased I_d. In Fig. 5.8(b), both channels showed SS of 70 mV/dec, and maximum dc g_m improved from 1.4 S/mm to 1.7 S/mm with increasing In content.

In the plot of $\sqrt{I_d}/g_m$ versus I_d in Fig. 5.8(c), the 80% In channel device presented lower values of $\sqrt{I_d}/g_m$ compared to the 65% In channel device. The improvement in the ratio of g_m/I_d was due to enhanced electron mobility in part. g_m also depends on the electron confinement in the channel. Fig. 5.9 shows the simulated conduction band edge and the electron density under the gate at 300 K. For the 80% In channel HEMT, the 2DEG was much closer to the gate which leads to a more efficient charge control.[32]

In Fig. 5.8(d), a pronounced impact ionization in the 80% In channel device was observed due to the relatively smaller bandgap for the higher In channel

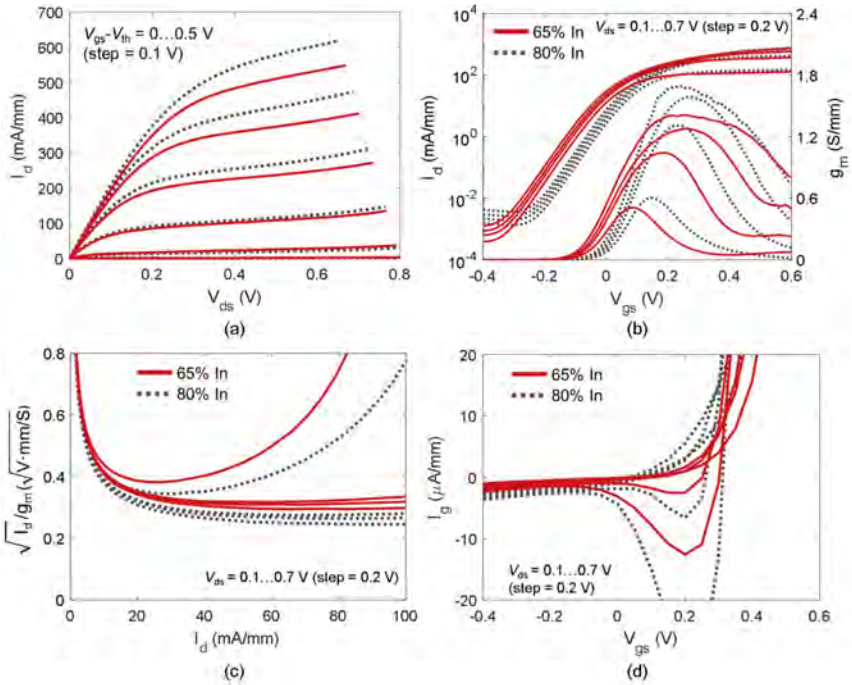


Figure 5.8: (a) I_d versus V_{ds} (b) I_d and g_m versus V_{gs}, (c) $\sqrt{I_d}/g_m$ versus I_d, and (d) I_g versus V_{gs} of the 65% In channel HEMT (solid) and the 80% In channel HEMT (dotted) at 300 K (Paper [E]).

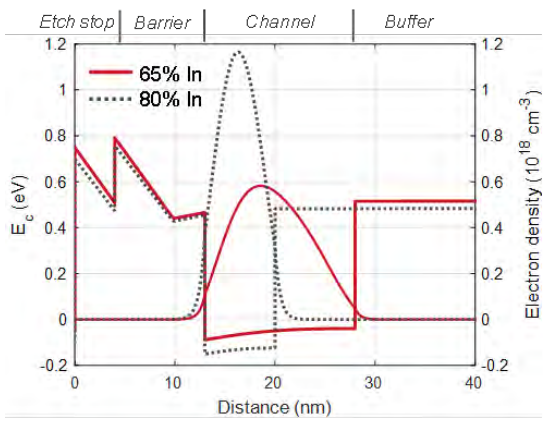


Figure 5.9: 1D simulation of the conduction band and the electron density under the gate of the 65% In channel (solid) and the 80% In channel (dotted) structure at 300 K from the Poisson-Schrödinger solver[75] (Paper [E]).

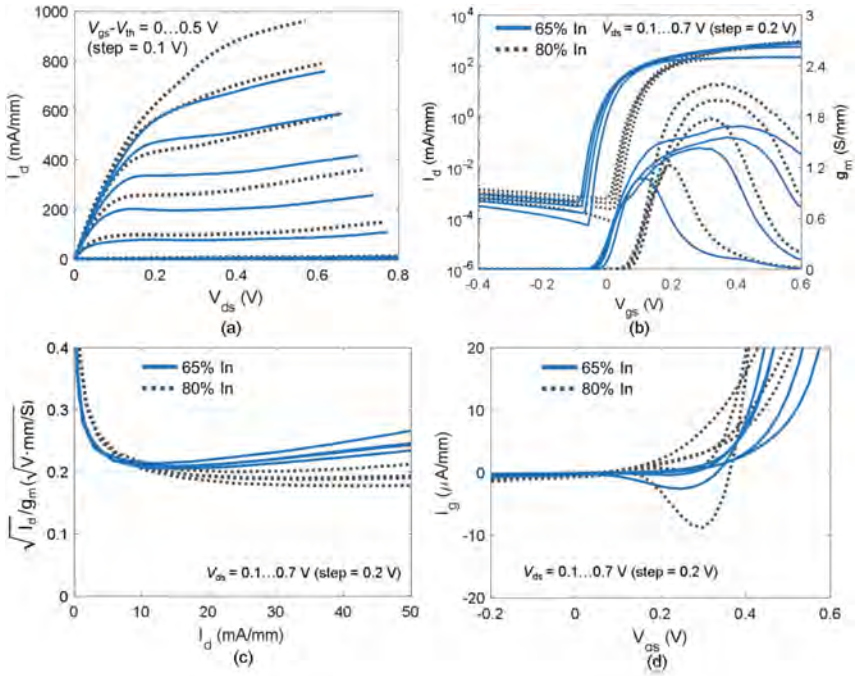


Figure 5.10: (a) I_d versus V_{ds} (b) I_d and g_m versus V_{gs}, (c) $\sqrt{I_d}/g_m$ versus I_d, and (d) I_g versus V_{gs} of the 65% In channel HEMT (solid) and the 80% In channel HEMT (dotted) at 5 K (Paper [E]).

content. The reverse I_g was about 0.1 μA/mm for both cases. Compared to the I_g of the InP HEMT using *structure A* in Chapter 4, I_g was reduced by a factor of 100 despite the 2 nm thinned barrier.

The dc characteristics at 5 K shown in Fig. 5.10 presented overall improvement for the 80% In channel HEMTs with respect to I_d and the maximum g_m (about 30% improvement). However, the 80% In channel HEMT showed a degraded SS (20 mV/dec for the 80% In, and 17 mV/dec for the 65% In channel HEMT). SS is related to the quality of the interface.[76,77] The difference in SS observed between the two In channel HEMTs may therefore be related to interface states or roughness in the heterostructure. Also, at cryogenic temperatures, the 2DEG confinement improves as the thermal energy of electrons decrease which in turn enhances the influence of interface states or traps.[32,39]

When the device is in the weak inversion condition, g_m to I_d ratio depends on SS.[45,70,71] Hence, the 80% In channel device resulted in higher values of $\sqrt{I_d}/g_m$ in the low I_d range (i.e. below 10 mA/mm) as plotted in Fig. 5.10(c). As I_d increased, $\sqrt{I_d}/g_m$ of the HEMT with higher mobility channel showed lower values, so generally improved noise performance for the high In content

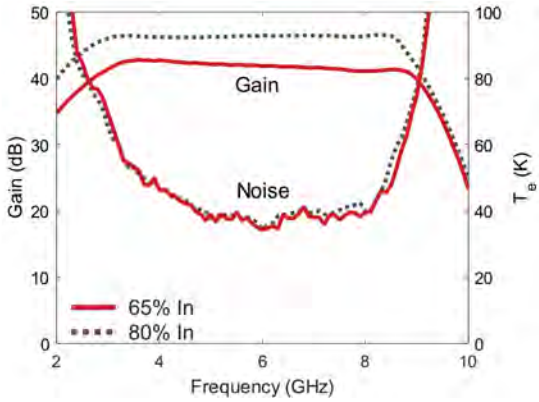


Figure 5.11: The measured gain and noise temperature of 4–8 GHz LNA integrated with two different channel HEMTs at 300 K. The LNAs were biased at $V_d = 1.35$ V and $I_d = 45$ mA (Paper [E]).

channel device is expected.

I_g at 5 K is plotted in Fig. 5.10(d). The reverse I_g at pinch-off was only about 50 nA/mm for both HEMTs. The measured I_g was in the order of 0.1 μA/mm for both devices at the optimum noise bias. The impact of I_g to the C−band LNA noise performance will thus be negligible as discussed in Paper [B].

5.2.2 HEMT noise properties

The impact of channel structures on noise performance was tested in a three-stage 4–8 GHz HEMT hybrid LNA.[10] HEMTs with $L_g = 100$ nm and $W_g = 2\times100$ μm were integrated for each stage. Fig. 5.11 shows the gain and T_e of LNAs with 80% In and 65% In channel HEMTs at 300 K. $T_{e,avg}$ of the 80% In channel HEMT LNA was 40 K with a gain of 46 dB. $T_{e,avg}$ of the 65% In channel HEMT LNA was 39 K with a gain of 42 dB. $T_{e,avg}$ for both channels showed comparable values at 300 K whereas a 4 dB higher gain was achieved in the LNA with 80% In channel HEMTs.

The 5 K measurements are shown in Fig. 5.12. At the optimal noise bias, the 80% In channel HEMT LNA exhibited a $T_{e,avg}$ of 2.4 K with 40 dB, and the 65% In channel HEMT LNA a $T_{e,avg}$ of 1.4 K with 39 dB. In Fig. 5.13, $T_{e,avg}$ and gain of two LNAs at various P_{dc} down to 300 μW are plotted. The 80% In channel HEMT LNA showed higher $T_{e,avg}$ than the 65% In channel HEMT LNA whereas the gain was almost the same for both structures.

To understand differences in noise performance of LNAs with two different channel HEMTs, the small-signal parameters were extracted at the optimal noise bias. As shown In Table 5.2, at 300 K, the higher In channel content improved $g_{m,i}$. However, both channels ended up with similar values of intrinsic

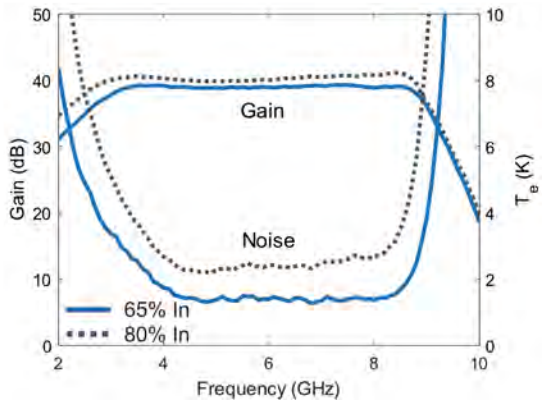


Figure 5.12: The measured gain and noise temperature of 4–8 GHz LNA integrated with two different channel HEMTs at 5 K. The LNAs were biased at $V_d = 0.5$ V and $I_d = 11$ mA (Paper [E]).

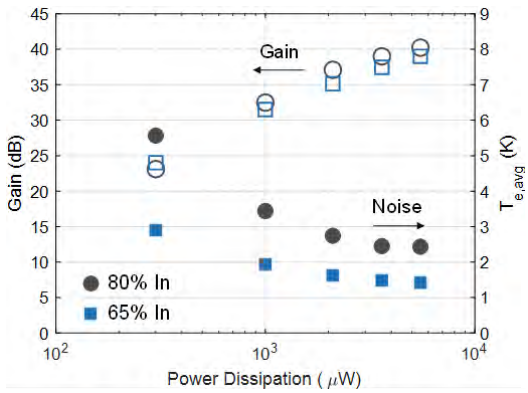


Figure 5.13: Gain and average noise temperature versus LNA dc power dissipation for 80% In (circle) and 65% In (square) channel InP HEMTs at 5 K (Paper [E]).

f_T due to a significant increase of C_{gs} and C_{gd} counteracting the improvement of $g_{m,i}$ resulting in the comparable f_T.

At 5 K, the improvement in $g_{m,i}$ from increased In channel content was much smaller than for 300 K whereas C_{gs} was significantly higher as seen in Table 5.2. Consequently, f_T for the 80% In channel HEMT was lowered. This is consistent with the results from dc g_m. In fact, the 80% In channel device exhibited improved maximum f_T (Paper [E]). This is because at the bias for maximum f_T (in strong inversion region), C_{gs} is saturated since 2DEG can not be populated in the barrier for both channels. Thus, the enhanced mobility channel can take advantage of the increase in $g_{m,i}$. However, at

Table 5.2: Intrinsic small-signal parameters, gate leakage current, and intrinsic cut-off frequencies of the InP HEMT at the optimum low-noise bias at 300 K and 5 K. Units are fF, mS, Ω, μA, and GHz (Paper [E]).

	300 K		5 K	
indium content	80%	65%	80%	65%
V_{ds}	0.64 V		0.33 V	
I_d	15 mA		3.67 mA	
C_{gs}	145	120	138	111
C_{gd}	35	28	46	40
C_{ds}	70	66	55	55
$g_{m,i}$	288	243	183	178
R_i	1.4	2.1	1.0	1.1
R_j	31	35	15	18
g_{ds}	15	17	12	17
I_g	0.5	0.2	0.05	0.02
f_T	231	238	156	172

the weak/moderate inversion region, f_T depends more on 2DEG confinement or the distance between the gate and 2DEG. This result indicates that the device optimized for the highest possible f_T does not lead to the lowest noise properties.

Fig. 5.14 presents C_{gs}, $g_{m,i}$, f_T, and extracted T_d and T_{min} as a function of LNA P_{dc} at 5 K. f_T for the 80% In channel HEMT was observed to be approximately 20% lower than the 65% In channel HEMT. This can be part of the reason to a 70% higher noise for the 80% In channel HEMT. Apart from f_T, T_d exhibited a distinct difference between the devices. T_d was almost 200% higher in the 80% In channel HEMT compared to the 65% In channel device. It is known that T_d is linearly dependent on I_d.[12,32] Since the two structures were characterized at the same L_g, W_g, and I_d in this study, the large difference in T_d is likely to be related to the intrinsic channel.

T_d can be understood as the noise from the turbulence or disturbance in the electron flow in the channel. The more the electrons are scattered, the more noisy the channel becomes. The scattering at cryogenic temperature is limited by alloy disorder and interface roughness scattering.[78–81] The alloy scattering depends on how much the electron wavefunction penetrates into the barrier.[78] The simulation in Fig. 5.9 shows a higher wavefunction amplitude in the InAlAs barrier. In addition, the degraded SS and $g_{m,i}$ for the 80% In channel HEMT is an indication of elevated interface roughness scattering. I. Watanabe *et al.* reported that the increased interface roughness in the InAlAs/InGaA heterointerface reduced the average electron velocity (v_e) at cryogenic temperatures.[82] From the delay time analysis presented in Paper [E], it was found that the 65% In channel HEMT showed an improved v_e at 5 K.

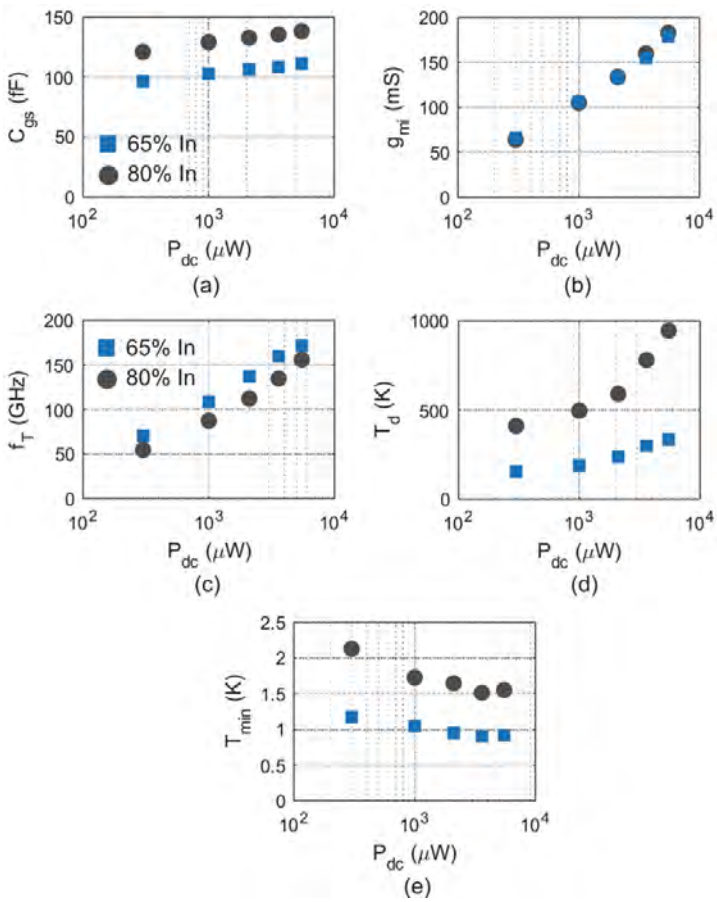


Figure 5.14: (a) gate-source capacitance, (b) intrinsic transconductance, (c) intrinsic cut-off frequency, (d) equivalent drain temperature, and (e) minimum noise temperature at 6 GHz as a function of LNA dc power dissipation for 80% In (black solid circle) and 65% In (blue solid square) channel HEMTs at 5 K (Paper [E]).

This study concludes that for the low-noise device design optimized for low-power cryogenic LNAs, the InP HEMTs must be optimized for as low as possible T_d and as high as possible f_T in the weak/moderate inversion region. To achieve that, HEMTs with a low SS and a high ratio of $g_{m,i}/C_{gs}$ are suitable.

5.3 Summary

The improved $g_{m,i}$ at low bias conditions was achieved using a very short gate-to-channel distance with respect to the 100 nm gate-length device while suppressing the gate leakage current. The 4−8 GHz LNA equipped with the InP HEMTs with the scaled barrier achieved $T_{e,min}$ of 2.4 K at 4.4 GHz with $T_{e,avg}$ of 2.8 K and gain of 26.9 dB at P_{dc} of 300 μW. When the LNA was biased for even lower P_{dc} of 112 μW, the LNA exhibited a $T_{e,avg}$ of 4.1 K and a gain of 20 dB. The demonstration of such low-power cryogenic C–band HEMT LNAs is of interest for the 4 K read out stage in future multi-qubit computing systems.

The effect of indium content in the InP HEMT channel on cryogenic noise properties has been studied. From a comparative study of $In_{0.65}Ga_{0.35}As$ and $In_{0.8}Ga_{0.2}As$ channels, the HEMT with lower indium channel content resulted in superior cryogenic C−band LNA noise performance at various dc power levels. This was a result of high f_T and low T_d from the lower In channel HEMT at the low-noise bias conditions. For the cryogenic low-power LNA, the low-noise InP HEMT designs needed to achieve a high ratio of $g_{m,i}/C_{gs}$ in the weak inversion region. In addition, T_d was suggested to a dominant effect for cryogenic HEMT noise properties.

Chapter 6

InP HEMT Design for Stable Cryogenic Operation

Abnormal cryogenic HEMT operation has been reported in several studies.[17,22–27] G. Moschetti *et al.*[26] reported that the four-finger metamorphic HEMT (mHEMT) exhibited a hysteretic change in the drain current, and a significant reduction in gain at cryogenic temperature. The observed instability was caused by a resonance induced by a drain feeder which connects two drain contacts in the four-finger transistor. In order to eliminate the resonances, an air-bridge was added across the drain which shifted the resonance frequency toward higher values beyond f_{max} of the mHEMT.

M. Varonen *et al*[22] proposed another solution for stable cryogenic HEMT operation. The four-finger HEMTs were divided into two discrete two-finger HEMTs. In this way, oscillations at several hundreds of GHz occurring within a four-finger device was avoided. The design technique proposed here assumed that the two-finger devices were stable at cryogenic operation. However, instability of the two-finger devices was not yet discussed. The problem was reported already in 1986.[27] The oscillations at several tens of GHz was noted, but the solution for instabilities was not found. A reliable and reproducible cryogenic LNA operation can only be obtained when a transistor operates in a stable manner. Hence cryogenic instability in two-finger InP HEMTs needs to be investigated more in detail.

In this chapter, the electrical stability of two-finger InP HEMTs is investigated at room and cryogenic temperature. Different stabilization solutions are experimentally demonstrated both on device and circuit level by cryogenic measurements.

6.1 HEMT stability characterization

The instability of various gate-widths, ranging between 10 μm and 100 μm, and gate-lengths, between 60 nm and 130 nm, of two-finger HEMTs at 300 K and 5 K was investigated. The HEMTs were fabricated using the epitaxial structure *A* shown in Fig. 3.1. The dc measurements were carried out with the drain voltage in steps of 25 mV and with the gate voltage in steps of 20 mV. The S-parameter measurements were carried out in a frequency range from 20 MHz to 60 GHz.

Fig. 6.1 presents the $I-V$ characteristics, g_m at V_{ds} =0.8 V and gain

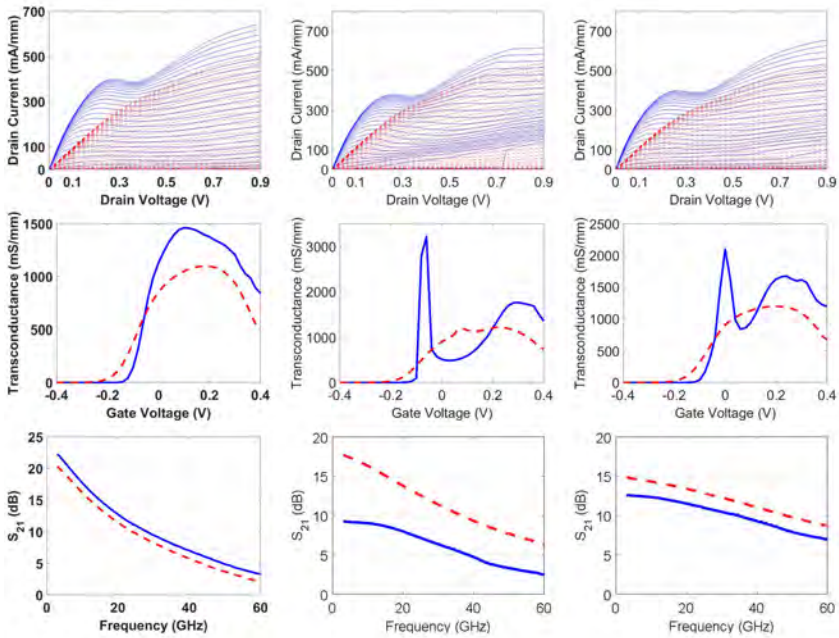


Figure 6.1: The $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $I_d = 190$ mA/mm of a 2×100 μm (left column), $2 \times 50\,\mu$m (middle column) and 2×30 μm (right column) 100 nm HEMTs at 300 K (red dashed) and 5 K (blue solid) (Paper [A]).

(S_{21}) measured at $V_{ds} = 0.8$ V and $I_d = 190$ mA/mm at 300 K and 5 K. The measured transistors were 2×100 μm, $2\times$ 50 μm, and 2×30 μm 100 nm gate-length HEMTs. At 300 K, the HEMTs showed a continuous drain current and transconductance regardless of the device sizes. Upon cooling, the devices with a small W_g, such as 2×50 μm and 2×30 μm, exhibited an abrupt increase in I_d and a large output conductance. Moreover, multiple peaks in g_m were observed, and the gain was lowered at 5 K in the instability region. However, the observed cryogenic instability did not appear in a larger W_g of 2×100 μm as shown in Fig. Fig. 6.1(a), or in an even smaller W_g, such as 2×10 μm and 2×20 μm HEMTs, which can be found in Paper [A]. It is important to mention that the 24–40 GHz (Ka–band) and 28–52 GHz (Q–band) MMIC LNA designs in this thesis utilize 2×30 μm and $2 \times 50\,\mu$m 100 nm gate-length HEMTs. Thus, the cryogenic instability observed in Fig. 6.1 must be mitigated for a reliable and reproducible cryogenic LNA performance.

The impact of the gate-length on cryogenic instabilities was studied. Fig. 6.2 compares the dc measurement results between two gate-lengths, 60 nm and 130 nm. Compared to the 100 nm process (see Fig. 6.1), the 60 nm gate-length HEMT exhibited even more unstable behavior at 5 K in terms

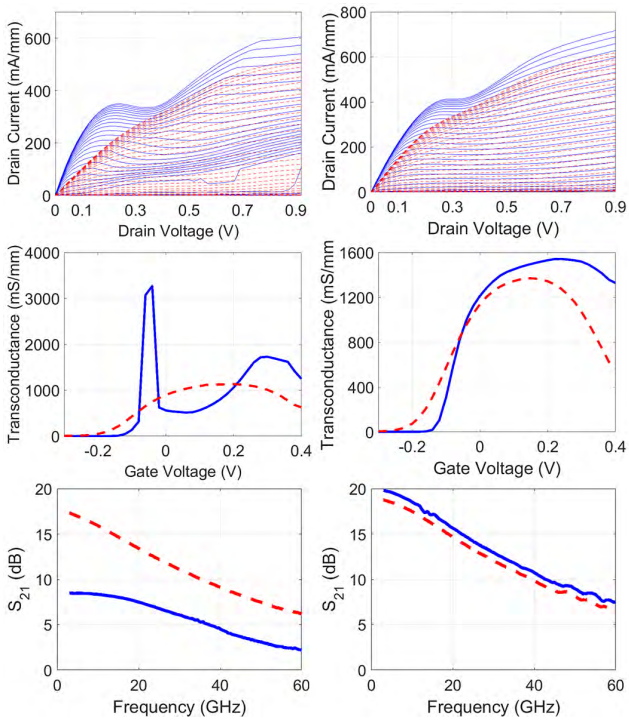


Figure 6.2: The HEMT $I-V$ characteristics, transconductance at $V_{ds} = 0.8\,\mathrm{V}$, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×50 μm at 300 K (red dashed) and 5 K (blue solid). The gate-length was 60 nm (left column) and 130 nm (right column) (Paper [A]).

of a wider inaccessible drain current region and a lower gain. On the other hand, as the gate-length increases to 130 nm, the two-finger HEMT showed stable characteristics both at 300 and 5 K similar to the one observed for the $2 \times 100\,\mu$m HEMT. The fact that the transistor with a shorter gate-length, and thus higher f_{max}, was more unstable, indicates that the instability can be related to oscillation at high frequencies as predicted by G. Moschetti *et al.*[26] and M. Varonen *et al.*[22]

M. Dyakonov and M. Shur predicted a current-induced instability in a gated 2DEG resulting in plasma generation in the terahertz range in 1993.[83] W. Knap *et al.* demonstrated terahertz emission appearing when I_d exceeded a certain threshold value.[84] The terahertz emission (0.4−1.0 THz) was caused by the drain current driven plasma instability, leading to terahertz oscillations in the channel. It was predicted that instability in the channel led to plasma waves, and the frequency of these waves depended on the electron concentration and the gate-length. More work is needed to figure out the relation between observed cryogenic instabilities and terahertz emission.

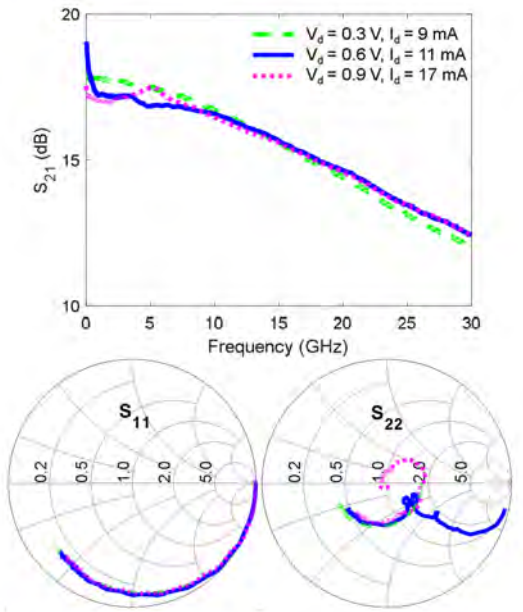


Figure 6.3: The S-parameter measurements of the 2×50 μm device with a 100 nm gate-length at $V_{ds} = 0.3$ V (green dashed), 0.6 V (blue solid), and 0.9 V (magenta dotted). $V_{gs} = 0$ V at an ambient temperature of 5 K (Paper [A]).

The rf cryogenic setup in this study only allowed measurements up to 67 GHz, so it was not possible to experimentally verify the high frequency resonances predicted by G. Moschetti *et al.*[26] and M. Varonen *et al.*[22] Instead, S-parameters were measured in a frequency range from 20 MHz to 67 GHz at 5 K. Fig. 6.3 presents the measured data up to 30 GHz where the abnormal features were observed. The bias point where the drain current suddenly increased is of particular interest. The HEMT with W_g of 2×50 μm and L_g of 100 nm HEMT was measured at 5 K using $V_{ds} = 0.3$, 0.6, and 0.9 V, and $V_{gs} = 0$ V. As seen in Fig. 6.1, the drain current jumps at around $V_{ds} = 0.7$ V. At a low drain drain bias of $V_{ds} = 0.3$ V, the S-parameters do not show any indication of instability. However, at $V_{ds} = 0.6$ V, which is right before the drain current jumps, the S-parameters start to deviate from the standard HEMT model. The S_{21} curve exhibits a spike at a few MHz and fluctuations around 5 GHz. In addition, in the S_{22} trace, an abnormal spike from 20 MHz to 10 GHz is observed. At a higher drain bias of $V_{ds} = 0.9$ V, the transistor oscillates where the drain current and output conductance suddenly increases. As seen in Fig. 6.3, the S_{21} curve fluctuates below 10 GHz at $V_{ds} = 0.9$ V. Fig. 6.3 also shows an inductive shift in S_{22} below 10 GHz which is mainly associated with impact ionization.[85,86] Similar dispersion in S-parameters in the low frequency range, in terms of an abnormal spike and ripples in S_{21},

was reported for four-finger InP HEMTs at cryogenic temperatures.[24] It was claimed that the dispersion observed at low frequencies was related to both the deep level traps in the buffer layer and oscillation.

The small-signal modeling at 300 K and 5 K could provide insight into the mechanism causing the instability. However, extraction of equivalent parameters was not possible since the bias condition fluctuated at an abnormal state. Hence the mechanism causing the cryogenic instability of two-finger InP HEMTs is not yet clear.

6.2 Design technique

In the layout of a multi-finger transistor, parallel fingers can induce signal mismatch at the edge of the gate.[24] Therefore, oscillations may occur due to the inherent asymmetry of the multi-finger transistor.[22,24] The two-finger transistor can be considered as two transistors placed in parallel, partially connected through grounded source contacts. One hypothesis is that the instability may arise when the two devices operate slightly out of phase. The phase difference may occur when two gates are asymmetric due to small variations in the process and from the asymmetry in the parallel source contacts. Thus, a stabilization solution which can make the parallel transistors to operate in phase should be tested. In this section, three different InP HEMT designs are presented in order to suppress the observed two-finger 100 nm gate-length HEMT instability at 5 K.

6.2.1 Source air-bridge

In order to stabilize the two-finger HEMT, an air-bridge was added across the two source contacts as shown in Fig. 6.4. By connecting the source contacts, the two parallel transistors were expected to have a stronger electric coupling.

Fig. 6.5 compares dc and rf measurements of the 2×30 μm and $2 \times 50\,\mu$m HEMTs with the source air-bridge at 300 K and 5 K. It shows that when adding the source air-bridge, abrupt steps in the drain current and discontinuities in the transconductance completely disappeared resulting in a largely enhanced S_{21}. These measurements clearly demonstrate that the cryogenic instability in the two-finger HEMT was eliminated with the source air-bridge. This is probably related to enhanced electric coupling between the two HEMTs.

6.2.2 Two gate fingers back-end connection

As an alternative way to enhance coupling between the parallel devices, the two gate fingers were connected at their back end with a thin metal strip forming a closed loop. Fig. 6.6 shows the modified layout by connecting the back end of gates. This method allows equalizing the potential at the two gates which in turn force the two parallel transistors to operate in phase.

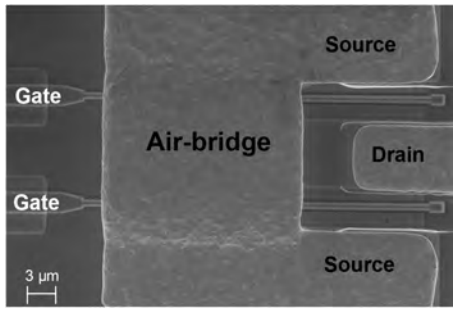


Figure 6.4: SEM image of a two-finger transistor with a source air-bridge (Paper [A]).

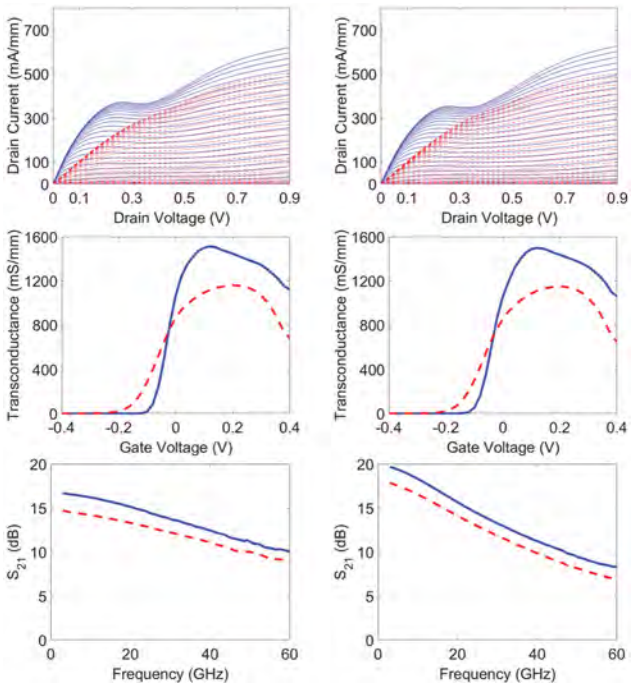


Figure 6.5: The $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×30 μm (left column) and 2×50 μm (right column) HEMTs with the source air-bridge. The measurements were done at 300 K (red dashed) and 5 K (blue solid) (Paper [A]).

The 2×30 μm and 2×50 μm HEMTs with two gates connected at the back end solution were measured at 300 K and 5 K and the results are shown in Fig. 6.7. This shows that the devices operated in a stable manner exhibiting the continuous drain current as well as transconductance, and a higher gain

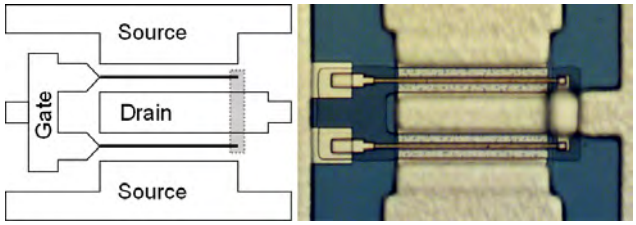


Figure 6.6: Modified layout (left) and micrograph (right) of a two-finger transistor by connecting the back end of the gates (Paper [A]).

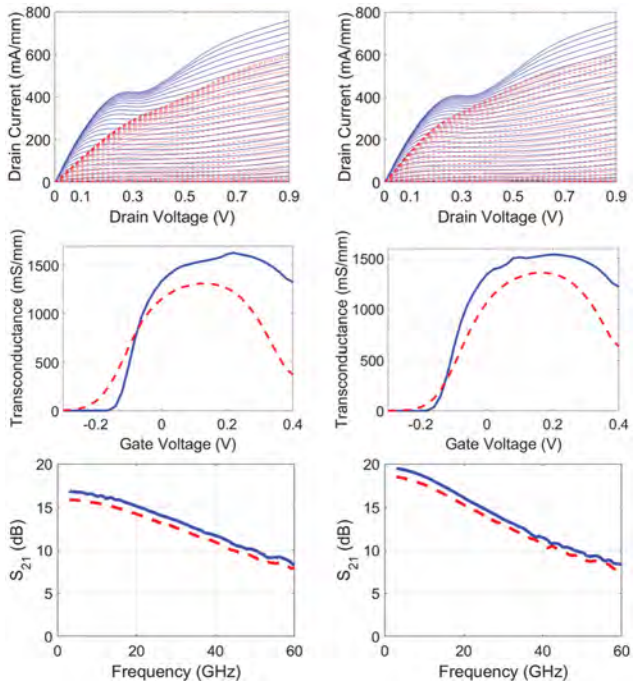


Figure 6.7: The $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×30 μm (left column) and 2×50 μm (right column) HEMTs with connecting the back end of gates. The measurements were done at 300 K (red dashed) and 5 K (blue solid) (Paper [A]).

at both temperatures. These measurements confirm that connecting gates at their back end also strengthens coupling between the two parallel devices which permits stable operation of the two-finger HEMT under cryogenic conditions.

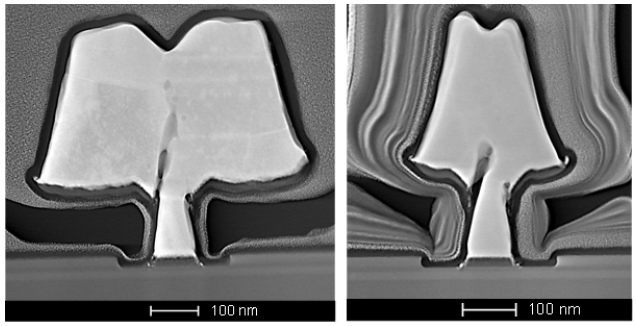


Figure 6.8: Cross-sectional STEM image of the HEMT with a gate resistance of 50 Ω/mm (left) and of 140 Ω/mm (right) (Paper [A]).

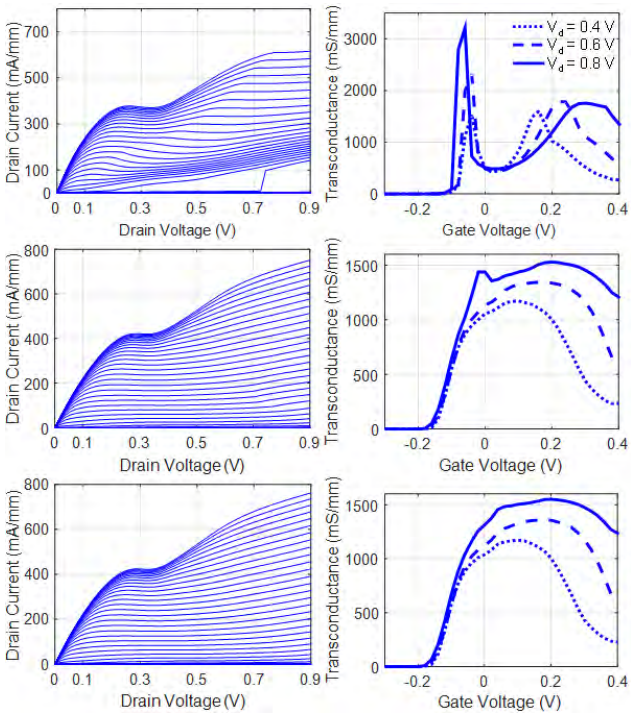


Figure 6.9: The $I-V$ characteristics and transconductance at $V_{ds} = 0.4$ V (dotted), 0.6 V (dashed), and 0.8 V (solid) of transistors with a 2×50 μm 100 nm HEMT. The gate resistance was 50 Ω/mm (top row), 90 Ω/mm (middle row) and 140 Ω/mm (bottom row) at 5 K (Paper [A]).

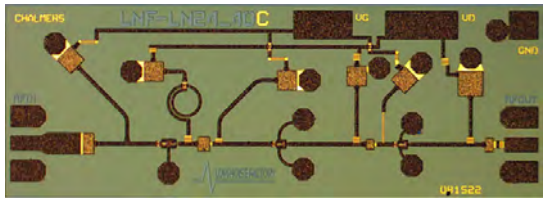


Figure 6.10: A photograph of fabricated three-stage 24–40 GHz MMIC HEMT LNA. The chip size was 2 mm × 0.75 mm (Paper [A]).

6.2.3 Gate resistance modification

As for the third solution, the effect of gate resistances was investigated. The idea behind this solution was that a higher gate resistance may attenuate potential oscillations within the device, resulting in stable operation of the two-finger InP HEMT at 5 K. In the standard process, the gate resistance was 50 Ω/mm at 5 K. The gate resistance was increased up to 140 Ω/mm by reducing the gate hat size. Fig. 6.8 displays the cross-sectional STEM images of two different gates.

Fig. 6.9 demonstrates the impact of the gate resistance on the cryogenic instability of the 2×50 μm HEMT. As the gate resistance was increased from 50 Ω/mm to 90 Ω/mm, the cryogenic instability was suppressed significantly showing a small peak in the transconductance curve only at a high $V_{ds} =$ 0.8 V. In the case of the HEMT with a higher gate resistance of 140 Ω/mm, the two-finger HEMT exhibited stable device characteristics regardless of V_{ds}. It confirms that the instability disappears by damping the oscillation by increasing the gate resistance. However, using a higher gate resistance is not a practical solution due to the fact that this solution strongly deteriorates HEMT noise performance.[12] Thus, either adding the source air-bridge or connecting two gates at the back end should be selected in order to effectively stabilize the two-finger devices for a cryogenic LNA.

6.3 MMIC LNA demonstration

Between the two solutions, either adding the source air-bridge or connecting two gates at the back end, a source air-bridge solution is preferred in the MMIC design. This is because the two source contacts are separated through via holes positioned about 50 μm away from the source when the source air-bridge is not present. Thus, the source air-bridge solution is necessary in order to avoid phase variation associated with the long interconnection. In this section, the stabilization effect of the source air-bridge technique is demonstrated in three-stage 24–40 GHz and four-stage 28–52 GHz MMIC LNAs. A photography of Ka–band LNA is presented in Fig. 6.10. The LNA included a 2×50 μm transistor for the first stage, and 2×30 μm transistors for the second and

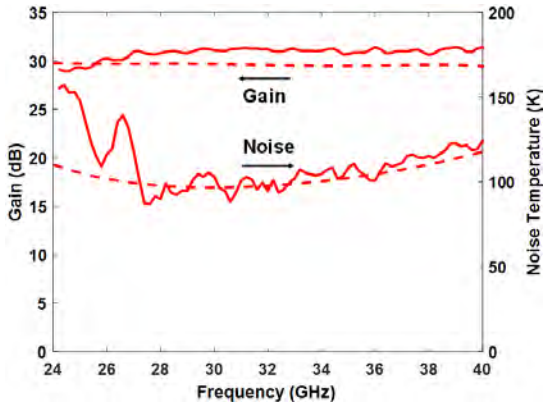


Figure 6.11: Simulated (dashed) and measured (solid) gain and noise temperature of the 24–40 GHz LNA at 300 K. The optimum noise bias for the LNA was $V_D = 1.2$ V, $I_D = 27$ mA (Paper [A]).

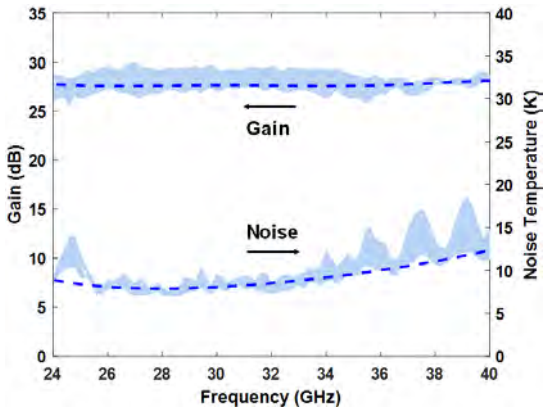


Figure 6.12: Simulated (dashed line) and measured (solid line and shaded area) gain and noise temperature of eight LNAs at 5.5 K. The optimum noise bias for the LNAs was $V_D = 0.5$ V, $I_D = 5$ mA (Paper [A]).

third stage. All transistors utilized the source air-bridge design.

The 24–40 GHz LNA was biased at $V_D = 1.2$ V and $I_D = 27$ mA at 300 K. As seen in Fig. 6.11, $T_{e,avg}$ was 110 K with $T_{e,min}$ of 87 K at 27.6 GHz, and the average measured gain was 31 dB.

When cooled down to 5.5 K, the LNAs were measured at the optimum noise bias of $V_D = 0.5$ V and $I_D = 5$ mA. Fig. 6.12 shows the measured and simulated noise temperature and gain of eight LNA chips. The LNAs exhibited $T_{e,avg}$ of 10.6 K with $T_{e,min}$ of 7 K at 25.6 GHz and the average measured gain of 29 dB. It also demonstrated the excellent uniformity of the LNA design with the source air-bridge solution along the wafer.

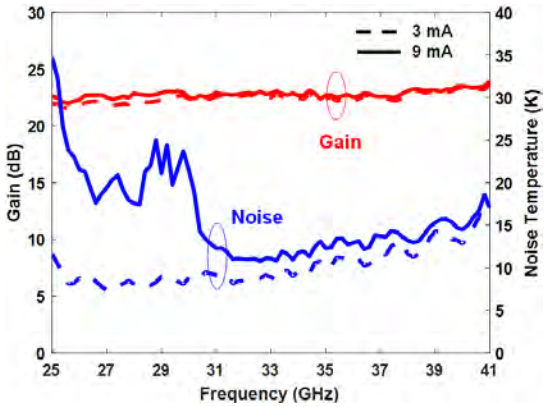


Figure 6.13: Measured gain and noise temperature of the MMIC LNA without the source air-bridge operating at 24–40 GHz at an ambient temperature of 5.5 K. The LNA was biased at $V_D = 1$ V, $I_D = 3$ mA (dashed) and 9 mA (solid) (Paper [A]).

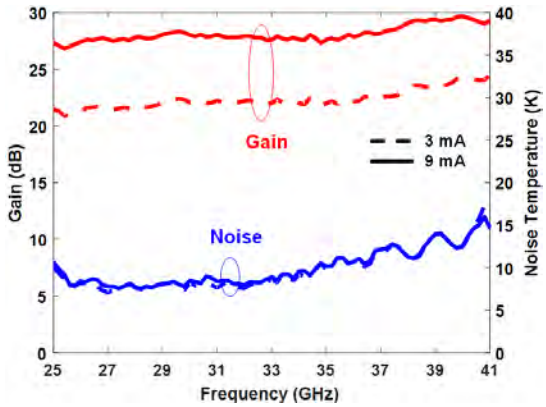


Figure 6.14: Measured gain and noise temperature of the MMIC LNA with the source air-bridge operating at 24–40 GHz at an ambient temperature of 5.5 K. The LNA was biased at $V_D = 1$ V, $I_D = 3$ mA (dashed) and 9 mA (solid) (Paper [A]).

Two versions of the MMIC LNA design in the Ka−band were fabricated: one with and one without the source air bridge for each transistor. This allowed the importance of HEMT stability at cryogenic operation to be seen. Figs. 6.13 and 6.14 show the measured noise temperature and gain of two variants at 5.5 K. The MMIC LNA with the non-stabilized HEMTs in Fig. 6.13 exhibited a drastic increase in the noise temperature as the drain current changed a small amount from 3 mA to 9 mA while the gain stayed at the same value of about 22 dB.

Table 6.1: State-of-the-art cryogenic Ka- and Q-band LNAs.

Ref.	Process	Freq. (GHz)	$T_{e,min}$	$T_{e,avg}$@T_{amb}(K)	Gain/Stage (dB)
5	0.1 μm InP HEMT	26−40	9.3	11.4@12	7.2
11	0.13 μm InP HEMT	24−40	10	13.2@15	9.3
60	0.1 μm GaAs mHEMT	25−34	-	15.2@15	8.1
87	80 nm InP HEMT	26−40	8	12.5@15	9
This work	0.1 μm InP HEMT	24−40	7	10.6@5.5	9.7
6	60 nm InP HEMT	35−50	-	13@20	7
88	70 nm GaAs mHEMT	33−50	13.5	18.4@15	6.8
89	0.1 μm InP HEMT	40−45	-	15@18	8.6
This work	0.1 μm InP HEMT	28−52	6.7	10@5.5	8.5

The 24–40 GHz LNA with the source air-bridge design was tested at the same bias conditions as shown in Fig. 6.14. When the drain current increased from 3 mA to 9 mA, the noise temperature was unchanged whereas only the gain increased from 22 dB to about 28 dB. The measurements in Figs. 6.13 and 6.14 clearly demonstrate the stabilization effect of the source air-bridge technique at the circuit level at cryogenic temperature.

The stabilization effect of the source air-bridge was also demonstrated in a four-stage 28–52 GHz MMIC LNA which presented $T_{e,avg}$ of 10 K with $T_{e,min}$ of 6.7 K at 32.8 GHz and the average gain of 34 dB at an ambient temperature of 5.5 K. Detailed circuit schematic, photo and LNA results at 300 K and 5.5 K can be found in Paper [A].

Table 6.1 compares the performance of the cryogenic HEMT MMIC LNAs of this work with previously reported LNAs, operating in similar frequency ranges and ambient temperatures.[5,6,11,60,87–89] The two cryogenic MMIC LNA design presented in this work both exhibited state-of-the-art performance in terms of the noise temperature, bandwidth as well as gain.

6.4 Summary

The cryogenic stability of two-finger 100 nm gate-length InP HEMTs was investigated. Electrical instabilities such as sudden changes in drain current

and sharp peaks in transconductance were observed at cryogenic temperature. The instability of two-finger HEMTs was mitigated by either adding a source air-bridge, connecting the back end of the gates, or increasing the gate resistance. The proposed source air-bridge technique was successfully demonstrated in a 24–40 GHz and a 28–52 GHz cryogenic InP HEMT MMIC LNA with a $T_{e,avg}$ of 10.6 K and 10 K, respectively.

Chapter 7

Conclusions and Future work

7.1 Conclusions

This thesis presented advances in InP HEMT technology optimized for low-noise, low-power dissipation, and electrical stability at cryogenic temperatures. The InP HEMT optimization was discussed in terms of the epitaxial layer design, fabrication, dc, rf, and noise characteristics. The noise performance of InP HEMTs was demonstrated in microwave and millimeter-wave cryogenic LNAs.

A 100 nm gate-length InP HEMT technology was developed by scaling barrier thickness to 8 nm. State-of-the-art cryogenic noise performance for wide-band MMIC LNAs was demonstrated with $T_{e,avg}$ of 3.5 K and 6.3 K for the 0.3−14 GHz and 16−28 GHz LNAs, respectively.

The impact of barrier scaling and channel composition of the InP HEMT on the noise temperature and dc power dissipation of the cryogenic LNA was studied. Through barrier scaling, the InP HEMT achieved an improvement of transconductance to drain current ratio at low drain voltages, which enabled a reduction of the power dissipation to 112 μW with $T_{e,avg}$ of 4.1 K in a 4−8 GHz LNA. From a comparative study of $In_{0.65}Ga_{0.35}As$ and $In_{0.8}Ga_{0.2}As$ channels, the InP HEMT with lower indium channel content resulted in superior cryogenic noise performance which was attributed to a reduced equivalent drain temperature as well as improved f_T under low-noise operation.

The cryogenic stability of two-finger InP HEMTs has been investigated. Unstable electric behavior in terms of jumps in drain current, discontinuous peaks in transconductance, and low-frequency dispersion in S-parameters was observed. The instability was associated with the partial connection between the two parallel transistors. Stabilization solutions which made the parallel transistors operate in phase were presented. By either adding a source air-bridge or connecting the back end of the gates, the device instability at cryogenic temperature was eliminated due to enhanced electric coupling between the two HEMTs. The instability was also suppressed by increasing the gate resistance which damped the oscillation. The source air-bridge solution was implemented in two cryogenic MMIC LNA designs in the frequency range of 24−40 GHz and 28−52 GHz, successfully demonstrating the electrically stabilized InP HEMTs at the circuit level. The $T_{e,avg}$ was 10.6 K and 10 K in the 24−40 GHz and 28−52 GHz InP HEMT MMIC LNAs, respectively.

7.2 Future work

In order to improve the InP HEMT noise performance under low-power operation, the InP HEMT technology should to be optimized for higher $g_{m,i}$ and f_T in the weak inversion region at cryogenic temperature. For that, a channel with high electron mobility and saturation velocity is needed. The InP HEMT with higher In channel content in Chapter 5 did not achieve an improvement in $g_{m,i}$ in the weak inversion region which was possibly due to elevated interface roughness scattering. In order to improve electron transport properties, a composite channel, such as a high indium content InGaAs layer inserted into a low indium content InGaAs layer, can be used. The composite channel has proven to minimize the interface roughness scattering, enhance the electron confinement in the insert layer, and improve the electron velocity.[90–92] The thickness and insertion position of the high indium content layer need to be optimized for improving $g_{m,i}$ and f_T under cryogenic low-noise operation.

The improvement in access resistance is essential for improving f_T. One way to lower the access resistance is by using a thick barrier which enable lower R_{sh} in the channel compared to a thin barrier layer. In this case, the gate-to-channel distance can be reduced by the Pt gate sink-in process. Pt gate metal thicknesses and annealing conditions need to be optimized for the lowest noise performance.

The channel structure is an important subject for further study. In Chapter 5, the indium channel content and the channel thickness were varied simultaneously, thus the differences in noise properties between the two channels were dependent on both parameters. In future research, a systematic change of the channel thickness with a specific channel composition, and vice versa, could be carried out in order to find the impact on the InP HEMT cryogenic noise properties.

Finally, the origin of the cryogenic instabilities in two-finger HEMTs needs to be better understood. Cryogenic measurements below 20 MHz may give more information regarding the low frequency dispersion as seen in Chapter 6, or alternatively by measuring S-parameters at several hundreds of GHz using a properly designed calibration substrate. In this way, potential resonances occurring for the cryogenic two-finger InP HEMT could be discovered.

Bibliography

[1] D. J. Mudgway and R. Launius, *Uplink-downlink: A History of the Deep Space Network 1957-1997*. National Aeronautics and Space Administration, 2001.

[2] J. Randa, E. Gerecht, D. Gu, and R. L. Billinger, "Precision measurement method for cryogenic amplifier noise temperatures below 5 K," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 3, pp. 1180–1189, 2006.

[3] J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P. A. Nilsson, J. P. Starski, N. Wadefalk, H. Zirath, and J. Grahn, "Ultralow-power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 664–666, 2012.

[4] M. W. Pospieszalski, "On the dependence of FET noise model parameters on ambient temperature," in *Radio and Wireless Symposium*, pp. 159–161, 2017.

[5] Y.-L. Tang, N. Wadefalk, M. A. Morgan, and S. Weinreb, "Full Ka-band high performance InP MMIC LNA module," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 81–84, 2006.

[6] M. Pospieszalski, S. Srikanth, K. Saini, B. Mason, and J. Effland, "ALMA Band 1 receiver development study," *9145A, Rev H1, National Radio Astronomy Observatory, Charlottesville*, 2013.

[7] M. Varonen, R. Reeves, P. Kangaslahti, L. Samoska, A. Akgiray, K. Cleary, R. Gawande, A. Fung, T. Gaier, S. Weinreb, A. C. S. Readhead, C. Lawrence, S. Sarkozy, and R. Lai, "A 75–116 GHz LNA with 23-K noise temperature at 108 GHz," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 1–3, 2013.

[8] E. W. Bryerton, X. Mei, Y.-M. Kim, W. Deal, W. Yoshida, M. Lange, J. Uyeda, M. Morgan, and R. Lai, "A W-band low-noise amplifier with 22 K noise temperature," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 681–684, 2009.

[9] L. Samoska, M. Varonen, R. Reeves, K. Cleary, R. Gawande, P. Kangaslahti, T. Gaier, R. Lai, and S. Sarkozy, "W-band cryogenic InP MMIC LNAs with noise below 30 K," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 1–3, 2012.

[10] N. Wadefalk, A. Mellberg, I. Angelov, M. E. Barsky, S. Bui, E. Choumas, R. W. Grundbacher, E. L. Kollberg, R. Lai, N. Rorsman, P. Starski,

J. Stenarson, D. C. Streit, and H. Zirath, "Cryogenic wide-band ultra-low-noise IF amplifiers operating at ultra-low DC power," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1705–1711, 2003.

[11] J. Schleeh, N. Wadefalk, P.-Å. Nilsson, J. P. Starski, and J. Grahn, "Cryogenic broadband ultra-low-noise MMIC LNAs for radio astronomy applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 2, pp. 871–877, 2013.

[12] M. W. Pospieszalski, "Extremely low-noise amplification with cryogenic FETs and HFETs: 1970-2004," *IEEE Microwave Magazine*, vol. 6, no. 3, pp. 62–75, 2005.

[13] M. Malmkvist, *Optimization of narrow bandgap HEMTs for low-noise and low-power applications*. PhD thesis, Chalmers University of Technology, Sweden, 2008.

[14] A. Leuther, A. Tessmann, M. Dammann, H. Massler, M. Schlechtweg, and O. Ambacher, "35 nm mHEMT technology for THz and ultra low noise applications," in *International Conference on Indium Phosphide and Related Materials*, pp. 1–2, 2013.

[15] W. R. Deal, K. Leong, V. Radisic, S. Sarkozy, B. Gorospe, J. Lee, P. H. Liu, W. Yoshida, J. Zhou, M. Lange, R. Lai, and X. B. Mei, "Low noise amplification at 0.67 THz using 30 nm InP HEMTs," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 7, pp. 368–370, 2011.

[16] D. Kim and J. A. del Alamo, "Lateral and vertical scaling of $In_{0.7}Ga_{0.3}As$ HEMTs for post-Si-CMOS logic applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2546–2553, 2008.

[17] J. Shell, "The cryogenic DC behavior of Cryo3/AZ1 InP 0.1-by-80-micrometer-gate high electron mobility transistor devices," *The Interplanetary Network Progress Report*, vol. 42–169, pp. 1–26, 2007.

[18] F. Danneville, G. Dambrine, H. Happy, P. Tadyszak, and A. Cappy, "Influence of the gate leakage current on the noise performance of MESFETs and MODFETs," *Solid-State Electronics*, vol. 38, no. 5, pp. 1081–1087, 1995.

[19] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. S. L. Brandão, D. A. Buell, B. J. Burkett, Y. Chen, Z. Chen, B. Chiaro, R. Collins, W. Courtney, A. Dunsworth, E. Farhi, B. Foxen, A. Fowler, C. Gidney, M. Giustina, R. Graff, K. Guerin, S. Habegger, M. P. Harrigan, M. Hartmann, A. Ho, M. Hoffmann, T. Huang, T. Humble, S. V. Isakov, E. Jeffrey, Z. Jiang, D. Kafri, K. Kechedzhi, J. Kelly, P. Klimov, S. Knysh, A. Korotkov, F. Kostritsa, D. Landhuis, M. Lindmark, E. Lucero, D. Lyakh, S. Mandrà, J. McClean,

M. McEwen, A. Megrant, X. Mi, K. Michielsen, M. Mohseni, J. Mutus, O. Naaman, M. Neeley, C. Neill, M. Y. Niu, E. Ostby, A. Petukhov, J. C. Platt, C. Quintana, E. Rieffel, P. Roushan, N. Rubin, D. Sank, K. Satzinger, V. Smelyanskiy, K. J. Sung, M. D. Trevithick, A. Vainsencher, B. Villalonga, T. White, Z. Yao, P. Yeh, A. Zalcman, H. Neven, and J. Martinis, "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, pp. 505–510, 2019.

[20] S. Montazeri and J. C. Bardin, "A sub-milliwatt 4–8 GHz SiGe cryogenic low noise amplifier," in *IEEE MTT-S International Microwave Symposium*, pp. 160–163, 2017.

[21] S. Montazeri, P. K. Grimes, C. E. Tong, and J. C. Bardin, "A wide-band high-gain compact sis receiver utilizing a 300-μw SiGe IF LNA," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–5, 2017.

[22] M. Varonen, R. Reeves, P. Kangaslahti, L. Samoska, J. W. Kooi, K. Cleary, R. S. Gawande, A. Akgiray, A. Fung, T. Gaier, S. Weinreb, A. C. S. Readhead, C. Lawrence, S. Sarkozy, and R. Lai, "An MMIC low-noise amplifier design technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 3, pp. 826–835, 2016.

[23] H. Sun and C. Bolognesi, "Anomalous behavior of AlGaN/GaN heterostructure field-effect transistors at cryogenic temperatures: From current collapse to current enhancement with cooling," *Applied Physics Letters*, vol. 90, no. 12, p. 123505, 2007.

[24] Q. Yang, "Low frequency dispersion in InP HEMTs," Master's thesis, Chalmers University of Technology, Sweden, 2013.

[25] M. W. Pospieszalski, S. Weinreb, R. D. Norrod, and R. Harris, "FETs and HEMTs at cryogenic temperatures-their properties and use in low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 3, pp. 552–560, 1988.

[26] G. Moschetti, F. Thome, M. Ohlrogge, J. Goliasch, F. Schäfer, B. Aja, A. Leuther, M. Schlechtweg, M. Seelmann-Eggebert, O. Ambacher, G. Wieching, and M. Kotiranta, "Stability investigation of large gate-width metamorphic high electron-mobility transistors at cryogenic temperature," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 10, pp. 3139–3150, 2016.

[27] M. W. Pospieszalski, "X-band noise performance of commercially available GaAs FETs at room and cryogenic temperatures," *Electronics Division Internal Report No. 260, National Radio Astronomy Observatory*, 1986.

[28] M. W. Pospieszalski, "Interpreting transistor noise," *IEEE Microwave Magazine*, vol. 11, no. 6, pp. 61–69, 2010.

[29] H. Hartnagel, R. Katilius, and A. Matulionis, *Microwave noise in semiconductor devices*. Wiley, 2001.

[30] M. W. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1340–1350, 1989.

[31] J. Schleeh, J. Mateos, I. Íñiguez-de-la-Torre, N. Wadefalk, P.-A. Nilsson, J. Grahn, and A. J. Minnich, "Phonon black-body radiation limit for heat dissipation in electronics," *Nature Materials*, vol. 14, no. 2, pp. 187–192, 2015.

[32] J. Schleeh, H. Rodilla, N. Wadefalk, P.-Å. Nilsson, and J. Grahn, "Characterization and modeling of cryogenic ultralow-noise InP HEMTs," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 206–212, 2013.

[33] M. W. Pospieszalski, "On certain noise properties of field-effect and bipolar transistors," in *International Conference on Microwaves, Radar & Wireless Communications*, pp. 1127–1130, 2006.

[34] A. Endoh, Y. Yamashita, K. Shinohara, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "InP-based high electron mobility transistors with a very short gate-channel distance," *Japanese Journal of Applied Physics*, vol. 42, no. 4B, pp. 2214–2218, 2003.

[35] T. Enoki, H. Ito, K. Ikuta, and Y. Ishii, "0.1 μm InAlAs/InGaAs HEMTs with an InP-recess-etch stopper grown by MOCVD," in *International Conference on Indium Phosphide and Related Materials*, pp. 81–84, 1995.

[36] G. Meneghesso, D. Buttari, E. Perin, C. Canali, and E. Zanoni, "Improvement of dc, low frequency and reliability properties of InAlAs/InGaAs InP-based HEMTs by means of an InP etch stop layer," in *International Electron Devices Meeting Technical Digest*, pp. 227–230, 1998.

[37] G. Meneghesso, R. Luise, D. Buttari, A. Chini, H. Yokoyama, T. Suemitsu, and E. Zanoni, "Parasitic effects and long term stability of InP-based HEMTs," *Microelectronics Reliability*, vol. 40, no. 8–10, pp. 1715–1720, 2000.

[38] H. Rodilla, J. Schleeh, P.-Å. Nilsson, and J. Grahn, "Cryogenic kink effect in InP pHEMTs: A pulsed measurements study," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 532–537, 2015.

[39] H. Rodilla, J. Schleeh, P. Nilsson, N. Wadefalk, J. Mateos, and J. Grahn, "Cryogenic performance of low-noise InP HEMTs: A Monte Carlo study," *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1625–1631, 2013.

[40] T. Suemitsu, T. Enoki, N. Sano, M. Tomizawa, and Y. Ishii, "An analysis of the kink phenomena in InAlAs/InGaAs HEMT's using two-dimensional device simulation," *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp. 2390–2399, 1998.

[41] T. Suemitsu, T. Enoki, H. Yokoyama, and Y. Ishii, "Improved recessed-gate structure for sub-0.1-μm-gate InP-based high electron mobility transistors," *Japanese Journal of Applied Physics*, vol. 37, pp. 1365–1372, 1998.

[42] [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/.

[43] G. Moschetti, *Ultra-Low Power InAs/AlSb HEMTs for Cryogenic Low-Noise Applications*. PhD thesis, Chalmers University of Technology, Sweden, 2013.

[44] G. Moschetti, N. Wadefalk, P. Åke Nilsson, Y. Roelens, A. Noudeviwa, L. Desplanque, X. Wallart, F. Danneville, G. Dambrine, S. Bollaert, and J. Grahn, "InAs/AlSb HEMTs for cryogenic LNAs at ultra-low power dissipation," *Solid-State Electronics*, vol. 64, no. 1, pp. 47–53, 2011.

[45] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley Sons, Inc., 2006.

[46] E. Cha, "InP high electron mobility transistor design for cryogenic low noise amplifiers," Licentiate thesis, Chalmers University of Technology, Sweden, 2018.

[47] H. Fourre, F. Diette, and A. Cappy, "Selective wet etching of lattice-matched InGaAs/InAlAs on InP and metamorphic InGaAs/InAlAs on GaAs using succinic acid/hydrogen peroxide solution," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 14, no. 5, pp. 3400–3402, 1996.

[48] M. Tong, A. A. Ketterson, K. Nummila, I. Adesida, L. Aina, and M. Mattingly, "Selective wet etching for InGaAs/InAlAs/InP heterostructure field-effect transistors," in *LEOS Summer Topical Meeting Digest on Broadband Analog and Digital Optoelectronics, Optical Multiple Access Networks, Integrated Optoelectronics, and Smart Pixels*, pp. 298–301, 1992.

[49] L. P. Sadwick, C. W. Kim, K. L. Tan, and D. C. Streit, "Schottky barrier heights of n-type and p-type $Al_{0.48}In_{0.52}As$," *IEEE Electron Device Letters*, vol. 12, no. 11, pp. 626–628, 1991.

[50] N. Harada, S. Kuroda, T. Katakami, K. Hikosaka, T. Mimura, and M. Abe, "Pt-based gate enhancement-mode InAlAs/InGaAs HEMTs for large-scale integration," in *International Conference Indium Phosphide and Related Materials*, pp. 377–380, 1991.

[51] K. Shinohara, W. Ha, M. Rodwell, and B. Brar, "Extremely high $g_m >$ 2.2 S/mm and $f_T > 550$ GHz in 30-nm enhancement-mode InP-HEMTs with Pt/Mo/Ti/Pt/Au buried gate," in *IEEE International Conference on Indium Phosphide and Related Materials*, pp. 18–21, 2007.

[52] T. Saranovac, A. Hambitzer, D. C. Ruiz, O. Ostinelli, and C. R. Bolognesi, "Pt gate sink-in process details impact on InP HEMT DC and RF performance," *IEEE Transactions on Semiconductor Manufacturing*, vol. 30, pp. 462–467, 2017.

[53] S. Kim, I. Adesida, and H. Hwang, "Measurements of thermally induced nanometer-scale diffusion depth of Pt/Ti/Pt/Au gate metallization on InAlAs/ InGaAs high-electron-mobility transistors," *Applied Physics Letters*, vol. 87, no. 23, p. 232102, 2005.

[54] K. Chen, T. Enoki, K. Maezawa, K. Arai, and M. Yamamoto, "High-performance InP-based enhancement-mode HEMTs using non-alloyed ohmic contacts and Pt-based buried-gate technologies," *IEEE Transactions on Electron Devices*, vol. 43, pp. 252–257, 1996.

[55] P. J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum f_T of millimeter-wave MODFETs," *IEEE Electron Device Letters*, vol. 10, no. 7, pp. 291–293, 1989.

[56] M. H. Somerville, A. Ernst, and J. A. del Alamo, "A physical model for the kink effect in InAlAs/InGaAs HEMTs," *IEEE Transactions on Electron Devices*, vol. 47, no. 5, pp. 922–930, 2000.

[57] T. Suemitsu, M. Tomizawa, T. Enoki, and Y. Ishii, "Enhancement of weak impact ionization in InAlAs/InGaAs HEMTs induced by surface traps: simulation and experiments," in *International Workshop on Computational Electronics*, pp. 250–253, 1998.

[58] G. Dambrine, A. Cappy, F. Héliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, pp. 1151–1159, 1988.

[59] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET's for millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 3, pp. 432–437, 1996.

[60] B. Aja Abelan, M. Seelmann-Eggebert, D. Bruch, A. Leuther, H. Massler, B. Baldischweiler, M. Schlechtweg, J. D. Gallego-Puyol, I. Lopez-Fernandez, C. Diez-Gonzalez, I. Malo-Gomez, E. Villa, and E. Artal, "4–12- and 25–34-GHz cryogenic mHEMT MMIC low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4080–4088, 2012.

[61] J. D. Pandian, L. Baker, G. Cortes, P. F. Goldsmith, A. A. Deshpande, R. Ganesan, J. Hagen, L. Locke, N. Wadefalk, and S. Weinreb, "Low-noise 6-8 GHz receiver," *IEEE Microwave Magazine*, vol. 7, no. 6, pp. 74–84, 2006.

[62] B. Aja, K. Schuster, F. Schafer, J. D. Gallego, S. Chartier, M. Seelmann-Eggebert, I. Kallfass, A. Leuther, H. Massler, M. Schlechtweg, C. Diez, I. López-Fernández, S. Lenz, and S. Turk, "Cryogenic low-noise mHEMT-based MMIC amplifiers for 4–12 GHz band," *IEEE Microwave and Wireless Components Letters*, vol. 21, pp. 613–615, 2011.

[63] M. W. Pospieszalski, E. J. Wollack, N. Bailey, D. Thacker, J. Webber, L. D. Nguyen, N. Le, and M. Lui, "Design and performance of wideband, low-noise, millimeter-wave amplifiers for Microwave Anisotropy Probe radiometers," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 25–28, 2000.

[64] R. J. Hussey, G. I. Sproule, J. P. McCaffrey, and M. J. Graham, "Characterization of oxides formed on InP, InGaAs, InAlAs, and InGaAs/InAlAs heterostructures at 300–500 °C," *Oxidation of Metals*, vol. 57, pp. 427–447, 2002.

[65] N. Newman, W. E. Spicer, T. Kendelewicz, and I. Lindau, "On the Fermi level pinning behavior of metal/III–V semiconductor interfaces," *Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena*, vol. 4, no. 4, pp. 931–938, 1986.

[66] M. Arps, H. . Each, W. Passenberg, A. Umbach, and W. Schlaak, "Influence of SiN_x passivation on the surface potential of GaInAs and AlInAs in HEMT layer structures," in *Proceedings of International Conference on Indium Phosphide and Related Materials*, pp. 308–311, 1996.

[67] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni, "30-nm two-step recess gate InP-Based InAlAs/InGaAs HEMTs," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1694–1700, 2002.

[68] W. T. Wong, M. Hosseini, H. Rücker, and J. C. Bardin, "A 1 mW cryogenic LNA exploiting optimized SiGe HBTs to achieve an average noise temperature of 3.2 K from 4–8 GHz," in *IEEE MTT-S International Microwave Symposium*, pp. 181–184, 2020.

[69] A. Beckers, F. Jazaeri, and C. Enz, "Theoretical limit of low temperature subthreshold swing in field-effect transistors," *IEEE Electron Device Letters*, vol. 41, no. 2, pp. 276–279, 2020.

[70] L. Barboni, M. Siniscalchi, and B. Sensale-Rodriguez, "TFET-Based circuit design using the transconductance generation efficiency g_m/I_d

Method," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 208–216, 2015.

[71] D. J. Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 1, pp. 8–14, 2004.

[72] I. Lopez-Fernandez, J. D. Gallego-Puyol, C. Diez, A. Barcia, and J. Martin-Pintado, "Wideband ultralow-noise cryogenic InP IF amplifiers for the Herschel mission radiometers," in *Millimeter and Submillimeter Detectors for Astronomy*, vol. 4855, pp. 489–500, SPIE, 2003.

[73] M. Malmkvist, S. Wang, and J. Grahn, "Epitaxial optimization of 130-nm gate-length InGaAs/InAlAs/InP HEMTs for low-noise applications," *IEEE Transactions on Electron Devices*, vol. 56, no. 1, pp. 126–131, 2009.

[74] C. S. Whelan, S. M. Lardizabal, P. M. Buhles, W. E. Hoke, P. F. Marsh, R. A. McTaggart, C. P. McCarroll, and T. E. Kazior, "A comparison of channel indium content in low noise metamorphic hemts with $In_xGa_{1-x}As$ (0.3<x<0.6)," in *Proceedings of International Conference on Indium Phosphide and Related Materials*, pp. 349–352, 2000.

[75] www.nextnano.de, *Next-nano simulation: software for electronics and optoelectronics semiconductor nanodevices.*

[76] B. Benbakhti, J. Ayubi-Moak, K. Kalna, and A. Asenov, "Effect of interface state trap density on the performance of scaled surface channel $In_{0.3}Ga_{0.7}As$ MOSFETs," *Journal of Physics: Conference Series*, vol. 193, p. 012122, 2009.

[77] Z. Tong, P. Ding, Y. Su, J. Niu, D. Wang, and Z. Jin, "Surface Improvement of InAlAs/InGaAs InP-Based HEMT Through Treatments of UV/Ozone and TMAH," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 600–607, 2020.

[78] D. Jena, *Polarization Effects on Low-Field Transport Mobility in III-V Nitride HEMTs.* Springer, 2008.

[79] D. Zanato, S. Gokden, N. Balkan, B. Ridley, and W. Schaff, "The effect of interface-roughness and dislocation scattering on low temperature mobility of 2D electron gas in GaN/AlGaN," *Semiconductor Science and Technology*, vol. 19, no. 3, pp. 427–432, 2004.

[80] G. Shin-ichirou, T. Kazuhiro, H. Masaomi, H. Chulun, and Y. Syoji, "Very high electron mobilities at low temperatures in $In_xGa_{1x}As/In_yAl_{1y}As$ HEMTs grown lattice-mismatched on GaAs substrates," *Journal of Crystal Growth*, vol. 201–202, pp. 749–752, 1999.

[81] F. Capotondi, G. Biasiol, D. Ercolani, and L. Sorba, "Scattering mechanisms in undoped $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ two-dimensional electron gases," *Journal of Crystal Growth*, vol. 278, no. 1, pp. 538–543, 2005.

[82] I. Watanabe, K. Shinohara, T. Kitada, S. Shimomura, A. Endoh, Y. Yamashita, T. Mimura, S. Hiyamizu, and T. Matsui, "Effects of heterointerface flatness on device performance of InP-based high electron mobility transistor," *Japanese Journal of Applied Physics*, vol. 46, no. 4B, pp. 2325–2329, 2007.

[83] M. Dyakonov and M. Shur, "Shallow water analogy for a ballistic field effect transistor: New mechanism of plasma wave generation by dc current," *Physical Review Letters*, vol. 71, pp. 2465–2468, 1993.

[84] W. Knap, J. Lusakowski, T. Parenty, S. Bollaert, A. Cappy, V. Popov, and M. Shur, "Terahertz emission by plasma waves in 60 nm gate high electron mobility transistors," *Applied Physics Letters*, vol. 84, pp. 2331–2333, 2004.

[85] R. Reuter, M. Agethen, U. Auer, S. van Waasen, D. Peters, W. Brockerhoff, and F.-J. Tegude, "Investigation and modeling of impact ionization with regard to the RF and noise behavior of HFET," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 6, pp. 977–983, 1997.

[86] W. Kruppa and J. Boos, "RF measurement of impact ionization and its temperature dependence in AlSb/InAs HEMTs," in *Proceedings of International Conference on Indium Phosphide and Related Materials*, pp. 339–342, 1994.

[87] M. W. Pospieszalski, "Cryogenic amplifiers for Jansky Very Large Array receivers," in *International Conference on Microwaves, Radar & Wireless Communications*, vol. 2, pp. 748–751, 2012.

[88] J. V. Terán Collantes, L. de la Fuente, B. Aja, and E. Artal, "Cryogenic broadband Q-band MMIC low-noise amplifier," in *European Microwave Integrated Circuits Conference*, pp. 77–80, 2016.

[89] M. Pospieszalski, W. Lakatosh, R. Lai, K. Tan, D. Streit, P. Liu, R. Dia, and J. Velebir, "Millimeter-wave, cryogenically-coolable amplifiers using AlInAs/GaInAs/InP HEMTs," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 515–518, 1993.

[90] T. Akazaki, K. Arai, T. Enoki, and Y. Ishii, "Improved InAlAs/InGaAs HEMT characteristics by inserting an InAs layer into the InGaAs channel," *IEEE Electron Device Letters*, vol. 13, no. 6, pp. 325–327, 1992.

[91] D. Kim and J. A. del Alamo, "Scalability of sub-100 nm InAs HEMTs on InP substrate for future logic applications," *IEEE Transactions on Electron Devices*, vol. 57, no. 7, pp. 1504–1511, 2010.

[92] D. Kim and J. A. del Alamo, "30-nm InAs pseudomorphic HEMTs on an InP substrate With a current-gain cutoff frequency of 628 GHz," *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 830–833, 2008.

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