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Enhanced Electrode Deposition for On-Chip Integrated Micro-Supercapacitors by Controlled Surface Roughening

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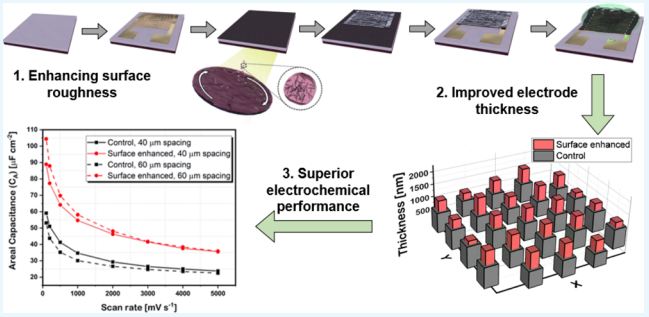
ABSTRACT: On-chip micro-supercapacitors (MSCs), integrated with energy harvesters, hold substantial promise for developing self-powered wireless sensor systems. However, MSCs have conventionally been manufactured through techniques incompatible with semiconductor fabrication technology, the most significant bottleneck being the electrode deposition technique. Utilization of spin-coating for electrode deposition has shown potential to deliver several complementary metal−oxide−semiconductor (CMOS)-compatible MSCs on a silicon substrate. Yet, their limited electrochemical performance and yield over the substrate have remained challenges obstructing their subsequent integration. We report a facile surface roughening technique for improving the wafer yield and the electrochemical performance of CMOS-compatible MSCs, specifically for reduced graphene oxide as an electrode material. A 4 nm iron layer is deposited and annealed on the wafer substrate to increase the roughness of the surface. In comparison to standard nonroughened MSCs, the increase in surface roughness leads to a 78% increased electrode thickness, 21% improvement in mass retention, 57% improvement in the uniformity of the spin-coated electrodes, and a high yield of 87% working devices on a 2″ silicon substrate. Furthermore, these improvements directly translate to higher capacitive performance with enhanced rate capability, energy, and power density. This technique brings us one step closer to fully integrable CMOS-compatible MSCs in self-powered systems for on-chip wireless sensor electronics.



1. INTRODUCTION

Intelligent wireless sensors are currently being used in several domains such as structural health monitoring through motion, strain, and temperature sensors;[1] physical and chemical sensing of biosignals;[2] damage detection in food and agriculture;[3] and in smartphones.[4] These sensors comprise four functional units—sensing, processing, communications, and a power unit. Powering these sensors is a critical issue that influences their application and architecture. Batteries are the standard method, but they restrict the device lifetime and incur costs for replacements.[5] Supercapacitors have demonstrated a higher power density and a longer life cycle compared to conventional batteries.[6] Supercapacitors are energy storage devices that generally use the physical separation of electrical charges in the electrode and electrolyte to store energy. Batteries could potentially be replaced by pairing on-chip supercapacitors called micro-supercapacitors (MSCs) with energy harvesters that convert energy from sources present in an ambient environment, such as thermal, vibrational, or acoustic energy.[7]

Successful integration of MSCs in a fully integrated circuit (IC)-compatible process scheme can lead to an on-chip power supply that will ease the power requirements of microsystems and improve their lifetime. A fully IC-compatible process requires some specific constraints regarding the choice of material and equipment for thin-film formation, photolithography, and etching.

MSCs have been fabricated through a variety of techniques such as chemical vapor deposition,[8,9] screen printing,[10] ink-jet printing,[11] laser scribing,[12] electrostatic spray deposition,[13] electrophoretic deposition,[14] chemical exfoliation,[15] doctor blade coating,[7] and spin-coating.[16] Spin-coating has the advantage of already being an established conventional part of standard metal−oxide−semiconductor (CMOS) processing, implying that it is as such inherently CMOS-/MEMS-compatible. Although ink-jet printing, spray-coating, and laser scribing can also be considered CMOS-compatible, there are several issues that need to be considered before they can provide effective wafer yield and high pattern resolution. Ink-jet printing, screen printing, and laser scribing

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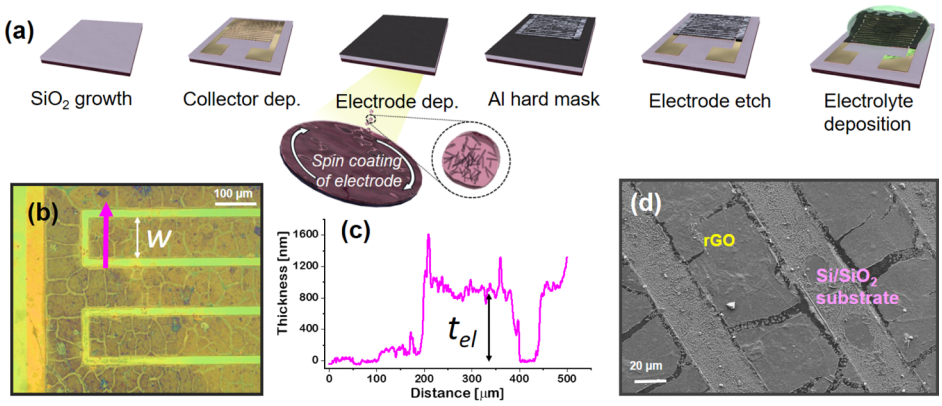

Figure 1. (a) Schematic process plan for the fabrication of spin-coated carbon-based MSCs on a silicon substrate fabricated through photolithography, (b) optical micrograph of the rGO electrode film on the Au/Ti/Fe contact pads, (c) conventional profile of the measured thickness of rGO electrodes and contacts on the MSC surface with 0 μ m starting from the lower end of the pink arrow in image (b), (d) scanning electron microscopy micrograph of the interdigitated electrodes at a 3 kV acceleration voltage at a 6 μA probe current in 8k× magnification.

have a raster scanning process which generates potential bottlenecks in the fabrication process. Recently, the tools for spray-coating have been set up in IC foundries owing to their flexibility in using various liquid solutions with varying properties and acquiring complex geometries, including high capacity for good step coverage.[17] However, the spray-coating equipment is complex and expensive and produces a high amount of waste solution. Also, recently, there have been some significant questions regarding the reproducibility and uniformity with more complex automation.[18] Chemical vapor deposition, one of the most promising techniques for CMOS-compatible processes, suffers from nonuniform wafer growth.[19] Thus, in view of the expected further automation in IC manufacturing,[20] its compatibility advantage makes spin-coating a strong candidate for being the preferred MSC manufacturing technique, provided it can demonstrate that it can produce devices of sufficient quality and yield.

In the past years, the focus on spin-coated MSCs for flexible substrates has increased substantially. Wu et al.[21] reported a flexible MSC with high energy density using water-dispensable graphene oxide (GO) with sulfonated polyaniline (GO/SP) as an electrode material through a combination of spin-coating, shadow masking, and plasma etching. The method demonstrated a thick GO/SP layer with a high volumetric capacitance. Similar efforts have been made for fabricating MSCs through shadow masking.[22−25] However, the use of a stencil shadow mask requires alignment precision that is performed manually. Similarly, Shen et al.[26] fabricated MSCs based on silica nanocomposites by pyrolysing a mixture of SU-8 thick photoresist and nanocomposites at 900 °C. The carbonization of photoresist to form thick electrodes has been termed as carbon-MEMS (C-MEMS).[27,28] Along with spin-coating, C-MEMS demonstrates the best potential of CMOS-compatible MSC fabrication. However, the pyrolysing temperature must be checked as most CMOS processes cannot go beyond a maximum temperature of 600 °C. More recently, Wu et al.[29] fabricated GO-based electrodes through spin-coating. The current collectors were evaporated on top of the spin-coated film through photolithography, followed by lift-off. Similar studies[30−32] have also utilized the spin-coating technique for MSC fabrication. The main issue with the deposition of current collectors on top is that the electrolyte penetration suffers, leading to a largely resistive behavior at high scan rates. In this regard, Smith et al.[33] demonstrate a feasible CMOS-compatible spin-coating fabrication technique that allows for electrolyte penetration in the entire electrode regions while having the current collectors at the bottom of the deposited electrode layer.

These spin-coated MSCs, however, suffer from poor adhesion and uniformity which leads to a poor performance with regard to charge retention as well as energy and power density. These parameters can be improved by enhancing the surface structure through substrate roughening. The primary effect of the surface structure on wettability has been established since the works of Wenzel[34] and Cassie and Baxter.[35] Both models have emphasized the improved wettability through surface roughness. This has been further modeled and experimentally described by Kubiak et al.[36] They concluded that surface roughness had a strong influence over the apparent contact angle of the spin-coated liquid, which improved the wettability. Similarly, Hsieh et al.[37] experimentally demonstrated an improved contact angle and surface coverage of oil-like fluid with the use of nanoparticles. Ryu et al. demonstrated an improved wettability on Si surfaces through linked copolymer coating of poly(methyl methacrylate) (PMMA) on the substrate.[38] Use of nonconductive PMMA between the current collectors and electrode layer will have a negative impact on the conductivity of the device. Therefore, solutions that improve the roughness of the substrate surface without affecting the device resistance are imperative. Monolayer colloidal crystals on Si and Au surfaces have also been recently used as surface roughness agents for etching and fabrication of super wet surfaces.[39] Furthermore, for improved structural control, techniques such as monodisperse polystyrene beads, nanoimprint lithography, and chemical etching have also been utilized to increase the roughness of a substrate surface.[40] MSCs fabricated on a rough surface by Vyas et al.[41] by annealing a thin hydrophilic film (Fe) below the current collectors combine the above-mentioned techniques to form a surface behaving as the nanoparticle layer. They have demonstrated equivalent capacitive behavior to the MSC fabricated on a smooth SiO_2 surface in initial measurements.

This paper focuses on these results for surface roughening through analysis of surface-enhanced and standard MSCs fabricated on separate 2″ Si substrates. The surface-enhanced (SE) Si substrate used for the fabrication of MSCs had an extra layer of Fe of 4 nm, annealed at a temperature of 600 °C for 4

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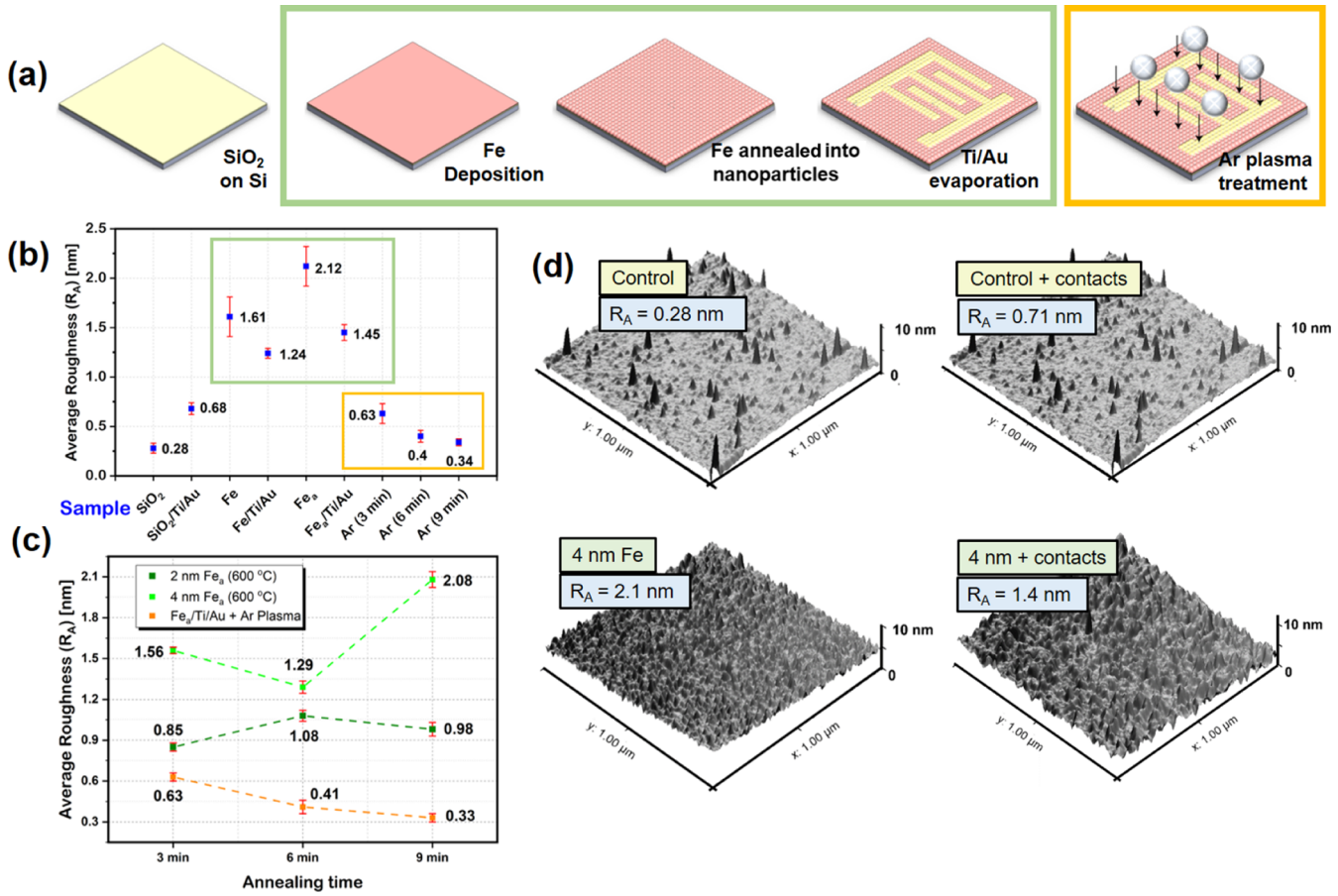

Figure 2. (a) Graphical process plan for the fabrication of Fe nanoparticles on a Si/SiO_2 substrate. The nanoparticles are prepared through evaporation of a thin Fe layer, followed by annealing at 600 °C. The current collector metals are then evaporated over the Fe-annealed layer. The schematic surfaces in green represent SE chips, and the chips in orange represent ArE chips. Average surface roughness of (b) various substrates in SPM Bruker Dimension (Digital Instruments, 3100) and (c) surface with the Fe layer of varying thickness annealed at 600 °C in the presence of Ar. (d) AFM micrographs of control and SE substrates demonstrating an increased surface roughness and retention after evaporation of Au/Ti contacts.

min to develop nanoparticles. MSCs were electrochemically analyzed, and the results demonstrate the better capacitive performance of the surface enhanced over standard MSCs in a range of devices with different electrode areas, all fabricated through a scalable CMOS-compatible process.

2. EXPERIMENTAL SECTION

2.1. Materials. The GO solution used for spin-coating was purchased from Graphene Supermarket. The solution was diluted with deionized (DI) water to 3 g/L and then sonicated for 15 min at 80 °C in 35 kHz sonication. The sonication before spin-coating dissociated the graphene platelets from stacking and aggregation. 1-Ethyl-3-methylimidazolium bis-(trifluoromethylsulfony)imide (EMIM-TFSI) was chosen as the electrolyte for two main reasons—first due to a higher operational window than aqueous electrolytes[42] and second due to its superior conductivity and electrochemical and thermal stability over other ionic liquid electrolytes.[43,44] Moreover, EMIM-TFSI has demonstrated a high energy density capability with graphene-based MSC electrodes.[45]

2.2. Surface Enhancement Study. A 2″ Si/SiO_2 substrate was diced into 1 cm × 1 cm chips. The chips were divided into three categories—SE, Ar-enhanced (ArE), and standard control (C) chips (kept unoptimized). SE chips had a Fe layer evaporated on them of different thicknesses—2, 3, and 4 nm. They were then annealed at 500, 600, 700, and 800 °C for 5 min each. The chips demonstrating the highest surface roughness were chosen for the evaporation of the current collectors. The ArE chips had an annealed Fe layer from the most roughened chip, that is, 4 nm thick layer annealed at 600 °C, with an Au/Ti layer evaporated on them. This was performed to emulate the actual fabricated device. They were prepared by treating the chips under an Ar plasma (40 sccm) in a PlasmaTherm ICP for 3−9 min with 1 min intervals. The Ar plasma in the process chamber was directed on the substrate with a radio frequency (RF) of 13.56 MHz at 100 W.

2.3. Fabrication of Reduced GO-Based MSCs. Figure 1a shows the schematic process plan for the MSC fabrication. Fabrication of the SE and control MSCs is performed on 2″ Si substrates with a 400 nm thermally grown layer of SiO_2. A 4 nm Fe layer was evaporated at a load pressure of 5×10^{-8} Torr using an e-beam evaporator (Kurt Lesker PVD225). The substrate was then annealed in a furnace at 600 °C for 5 min with a load−unload temperature of 150 °C and a 10 °C/min ramp-up temperature. A positive resist, S-1813 (micro-resist technology Gmbh), was spin-coated on the two substrates, SE and control, and then UV-exposed with a repromask designed for the MSC current collectors. The current collector metals, Au/Ti, were evaporated for thicknesses of 100 and 20 nm, respectively. The Ti metal film acts as an adhesion promoter

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ACS Omega 2020, 5, 5219−5228

and a diffusion barrier. The photoresist was lifted off in an mr-REM400 remover (micro-resist technology Gmbh) under the ultrasonication of 35 kHz in 55 min. GO was then spin-coated on the two substrates at an angular velocity of 1000 rpm with an acceleration of 1000 rpms for 60 s. This spin-coating process was repeated five times at the same velocity and acceleration. After subsequent spin-coatings, the spin-coated solution was hard baked in a 100 °C oven. Furthermore, a layer of Al of 70 nm was evaporated on the GO-laden substrates. The thin Al film served as a hard mask for etching the GO material from the inverse interdigitated pattern after a lithography step using photoresist S1813 (Rohm and Haas Electronic Materials). The exposed Al was etched using a mixture of Cl_2 and $SiCl_4$ with Ar gas as a catalyst for the reaction in the dry-ICP plasma (Oxford Systems). The exposed GO was then etched by O_2 flowing at 80 sccm with an RF power of 100 W. Finally, the Al hard mask was removed by etching the 70 nm film using the same gas mixture as before. A laser camera was set up over the ion etching tool to end the Al etch automatically as soon as the laser detected the GO surface. The end point is measured by the intensity of the reflected laser. As soon as the reflective Al surface is etched, the intensity of the reflected wave drops, denoting the end of Al etching. This process took approx. 6 min for etching. The GO underneath the hard mask was annealed in a high-temperature furnace at 600 °C for 5 min with the same ramp-up and -down temperatures as the Fe-annealing step. The fabricated substrates were then diced for individual MSC performance analysis using EMIM-TFSI as the electrolyte. Figure 1b shows the interdigitated electrodes of one of the fabricated MSCs.

2.4. Device Design. The fabricated substrates had several MSC designs based on the number of fingers and distances between them. The naming convention in the paper is *n*F-*d*, where *n* is the number of fingers and *d* is the spacing between the positive and negative electrodes in micrometers. The total material surface area for all the designs is 0.21 cm^2, while the total active surface area for the electrodes varies with the width (w) and d. The thickness of the electrodes is assigned as t_{el}. An in-depth study for control MSCs on a SiO_2 substrate has been performed by Li et al.[46]

2.5. Process Characterization. The roughness of all the samples for the surface enhancement experiments was analyzed using an atomic force microscope (SPM Bruker Dimension, 3100) in a 1 μm × 1 μm window. The mean roughness of the surface (R_A) was analyzed through a tapping mode with a cantilever of 285 kHz resonance frequency. R_A is the arithmetic average of the absolute values of the profile height deviations from the mean line, recorded within the evaluation length.

The fabrication process of the C- and SE-MSCs was analyzed using an optical microscope (Olympus SZH-11) during fabrication. The quality of the GO material was analyzed using a Raman microscope with a 638 nm laser and a spectrometer with 1200 lines/mm gratings. The Raman spectrum of the material after the reduction process shows two major features, the G band due to the E_{2g} symmetry of sp^2 carbon at 1587 cm^{-1} and the D band corresponding to the breathing mode of the A_{1g} symmetry at 1338 cm^{-1}. The intensity ratio of D to G band (I_D/I_G) is 1.39, similar to a previous report on reduced GO (rGO).[47] The thickness of the spin-coated rGO layers on the fabricated substrates was measured using a Dektak surface profiler. The surface morphologies of the devices were measured using a scanning electron microscope (JSM-7610F Schottky field emission), shown in Figure 1d at a scanning acceleration voltage of 1−5 kV with a probe current of 6 μA.

2.6. Electrochemical Measurement. The MSCs fabricated with the SE and C substrates were evaluated on a Karl Süss PM 5 probe station coupled with a Gamry Reference 3000AE potentiostat. Cyclic voltammetry (CV) at scan rates of 20−5000 mV s^{-1} is shown in Figure 4a,b. The total

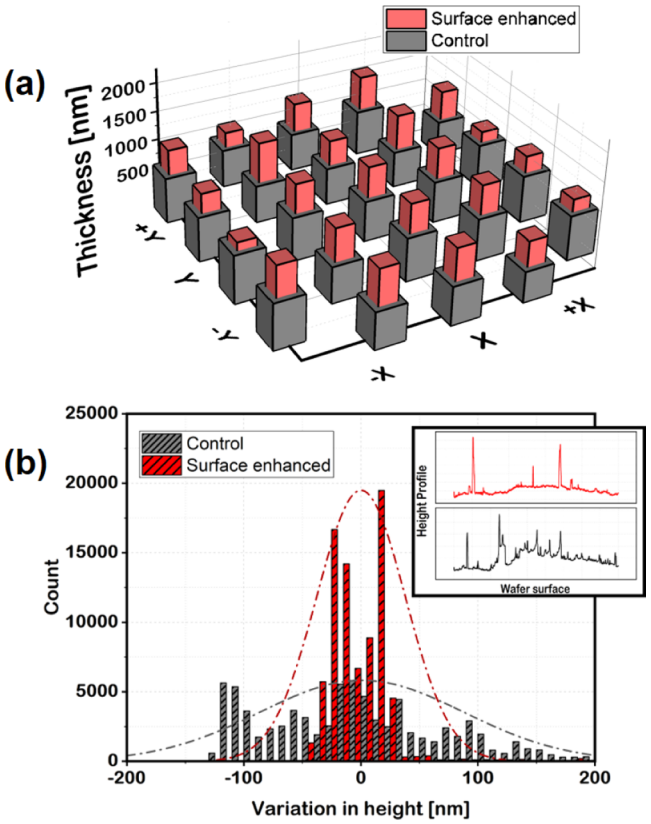

Figure 3. (a) Graphical representation of the measured thicknesses of the electrodes fabricated on the C- and SE-MSCs on a 2 × 2 in. substrate. (b) Histogram of the thickness distribution over the two substrates. Inset: representative 1 mm length evaluation of the surfaces with a Dektak Profiler.

capacitance of the devices was measured by calculating the total charge over the voltage window of the electrolyte using

$$C_t = \frac{\int i \, dt}{\Delta V} \quad (1)$$

where C_t is the total capacitance of the device, i is the current density, and ΔV is the voltage window of the electrolyte. Similarly, the areal capacitance C_a of the MSCs is calculated by normalizing C_t with the active electrode area (A)

$$C_a = C_t/A \quad (2)$$

The volumetric capacitance is calculated as

$$C_V = \frac{C_t}{A \times t_{el}} \quad (3)$$

The areal energy density is then calculated from C_a by

$$E = \frac{1}{2} C_a V^2 \quad (4)$$

From E, the power density of the MSC is

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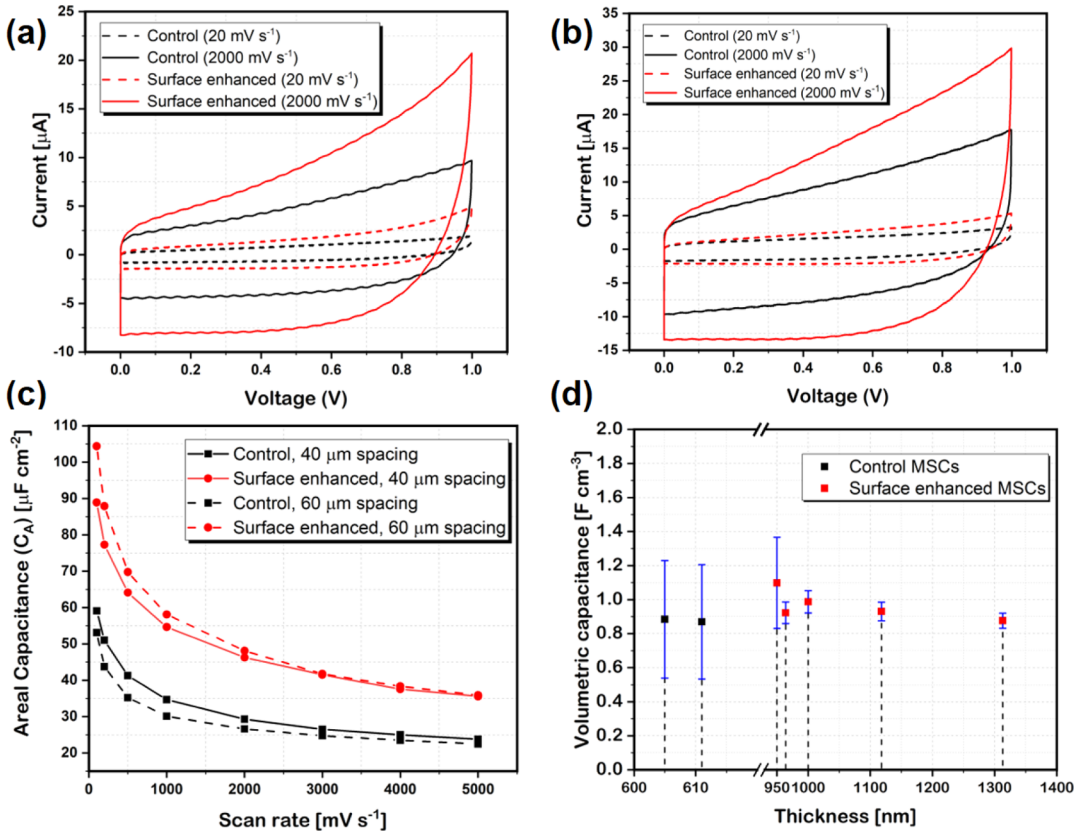

Figure 4. Cyclic voltammograms of (a) 20F-40 and (b) 20F-60 MSCs measured with a Gamry potentiostat. (c) Comparison of areal capacitances over increasing scan rates and (d) volumetric capacitance with respect to the thickness for C- and SE-MSCs with error bars calculated from error in thickness measurement and surface uniformity approximations.

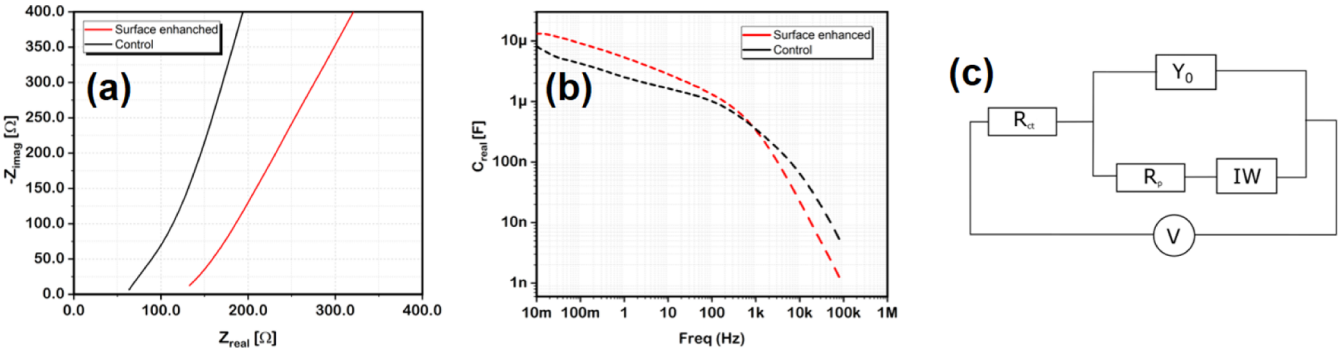

Figure 5. (a) Nyquist plot of 20F-40 and (b) real part of specific capacitance C_t at various working frequencies calculated from the Bode plot through impedance spectroscopy of C- and SE-MSCs. (c) Equivalent circuit model acquired from parametric fitting in impedance spectroscopy.

$$P = \frac{E}{t} \tag{5}$$

where t is the discharging time. Figure 5a shows the Nyquist plot of the SE- and C-MSCs. The electrolyte resistance of a MSC is calculated by finding the intercept of Z_{real} versus $-Z_{imag}$ curve on the Z_{real}-axis.

3. RESULTS AND DISCUSSION

3.1. Surface Roughening Results. Figure 2a shows the schematic process steps to induce surface roughening on samples. SE chips are illustrated in the green box, while the ArE chips are illustrated in orange. Figure 2b shows the R_A values of chips with different roughening processes. A control SiO_2 surface has the lowest R_A = 0.28 nm. When a layer of Au/Ti is evaporated over it, the roughness increases because of process-related parameters for such metal evaporation. Among the SE chips, an evaporated Fe thin film of 4 nm exhibits an R_A = 1.61 nm. When annealed at 600 °C for 9 min, the same film roughens to R_A = 2.12 nm. There is an observed reduction in R_A for both films upon evaporation of Au/Ti contacts of 100/20 nm, respectively. However, the annealed Fe sample (Fe_a/Ti/Au) shows a 16% improvement in R_A over the nonannealed sample (Fe/Ti/Au). The ArE chips after Ar plasma treatment at 100 W for 3, 6, and 9 min, respectively, showed a reduction in R_A by 56% for the lowest time and decreases ever further when Ar plasma is applied for higher times. Therefore, using plasma treatment for improving the R_A was discontinued. Figure 2d shows the atomic force microscopy (AFM) micrographs of the fabricated MSC surfaces after the lift-off

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process. The roughness of the control surface is the lowest at 0.28 nm, followed by the control and contact surface. The R_A for the SE samples is much higher than that for the control surfaces. Moreover, R_A of the contacts over the annealed Fe is also higher than the control + contact surface. Thus, the surface roughness of the Fe nanoparticles is preserved even after evaporation of the current collector. ArE chips, on the other hand, demonstrate that the use of Ar plasma over the roughened surface of Fe_a/Ti/Au reduces R_A by over 0.82 nm.

Figure 2c further illustrates the difference between the surface roughening techniques. The annealing process transforms the thin Fe film into nanoislands, while the Ar-plasma actions lead to a smoothening effect on the substrate surface. The 4 nm Fe layer, among the SE chips, demonstrated an R_A value of 2.1 ± 0.2 nm. Because the 4 nm Fe film annealed at 600 °C for 9 min demonstrated the highest R_A, this methodology was chosen for inducing roughening in the MSC fabrication process in order to improve the thickness and uniformity of the spin-coated GO electrodes. It is possible to achieve the same surface roughness in the Fe nanoparticle layer if we use a 2 nm Fe film at 500 °C for 5 min (AFM results in the Supporting Information). It is possible to scale down temperatures and achieve the same surface roughness in the Fe nanoparticle layer if we use a 2 nm Fe film annealed at 500 °C for 5 min (AFM results in the Supporting Information), which would move us further toward CMOS compatibility, for example, in Al-containing processes.

One of the major issues with the control substrate was in the nonuniformity of deposition during spin-coating. The topmost substrate on the control substrate is SiO_2,[48] which is hydrophobic. When the solution is poured over the substrate and spin-coated, the GO droplets would tend to coalesce into larger droplets with increased surface tension. With the angular velocity of the spinner, these droplets would move away from the completely hydrophobic surface. Therefore, the spinner tries to get rid of as much as possible of the GO solution which is composed of 90% DI water. The Fe-annealed nanofilm, on the other hand, is hydrophilic.[49] With such a mixed composition of hydrophilic Fe surface and hydrophobic Au surface,[50] the water composition of the spin-coated mixture is attracted toward the hydrophilic surface, leaving the residue on the hydrophobic Au surface. Adhesion of the spin-coated GO flakes on the SE substrate leads to a larger surface coverage on the substrate compared to that on the C substrate. The adhesive property of the SE substrate was observed while spin-coating the GO. The improved roughness led to a higher surface coverage in the first run of spin-coating. This single layer deposition was uniform across the entire substrate, that is, from the center to the edges. Thus, the deposition of a Fe layer leads to greater retention of GO solution on the substrate during the spin-coating process.

Figure 3a shows the improvement of thicknesses on the SE substrate over the control substrate. There is a 67% improvement in the thickness at the center, with the SE electrode at 1.07 μm compared to 0.64 μm on the control. At the edges, the retention on the SE substrates is more prominent with a 78% increased electrode thickness on an average over the control substrate, as can be seen in $\pm X$ ends. The devices on the SE substrate exhibited an average height of 1.16 μm, while the devices on the control had a height of 0.71 μm. The highest t_{el} = 1.26 μm is measured in the $-X + Y$ quadrant on the SE substrate, while the lowest t_{el} = 0.98 μm was found to be at the left edge of the $-X - Y$ quadrant.

Furthermore, there is a 21% improvement in the mass of the retained GO flakes on the SE substrate compared to that on the C substrate. This has previously been demonstrated in research conducted by Vyas et al.[41] As noted previously, the roughness induced by the annealing process leads to a higher coefficient of friction. Thus, with the optimal frictional coefficient for a SE sample, the GO flakes will tend to adhere to the wafer substrate.

The uniformity of the spin-coated GO over the substrate surface was analyzed by measuring several 1 mm windows over the substrate. Figure 3b shows the histogram of the thickness of the spin-coated GO on the control and SE surface. The graph shows that the uniformity of both the surfaces was interpreted as Gaussian distributions. The standard deviation on the SE is much lower than that of the control surface, that is, 37−87 nm.

3.2. Electrochemical Results. After fabrication, the MSCs on the two substrates, control (C-MSCs) and SE (SE-MSCs), were analyzed for their electrochemical performance with the EMIM-TFSI electrolyte. There were 23 devices on each of the SE and C substrates. Out of them, 20 devices on the SE substrate and only 8 devices on the C substrate demonstrated capacitive behavior when they were tested with EMIM-TFSI. The wafer yield of SE-MSCs is 87% compared to the meagre 33% for the C-MSCs. There was a resistive behavior observed on the remaining samples on both the substrates. All the devices with variable fingers and spacings, namely, 1F-40, 5F-40, 10F-40, 20F-40, and 20F-60, demonstrated similar behavior for SE- and C-MSC substrates, respectively. The scope of the results is currently to demonstrate the main differences in the performance of the C- and SE-MSCs.

Figure 4 shows a representative image of only two of the several devices fabricated on a 2 in. Si substrate. The analytical dependence of the number of fingers and spacings has previously been studied by Li et al.[46] They concluded that 20F-40 devices demonstrated the highest rate capability among all designs. Rate capability was measured by the ratio of high scan rate capacitance to low scan rate capacitance or similarly high current density capacitance to low current density capacitance. However, the performance of these devices on the edge of the substrates had demonstrated a higher drop in capacitance in comparison to other devices such as 1F-40 and 5F-40. This was in direct contradiction with the performance recorded for the devices in the center of the substrate. One of the main reasons for poor performance of the devices fabricated near the substrate edge was ineffective mass loading in the control substrate during spin-coating. As discussed in Section 3, SE produces a substantial improvement in the thickness of the electrodes, mass loading of GO, and uniformity of the spin-coated GO when the SE method is used.

Figure 4a,b shows the cyclic voltammograms of two of the fabricated MSCs on substrates, namely, 20F-40 and 20F-60, for both the C and SEdevices at 20 and 2000 mV s^{-1}, respectively. Both the devices reveal quasi-rectangular voltammograms that demonstrate a stronger influence of the capacitive behavior over resistive behavior in the MSCs. The charge retention capacity in both 20F-40 and 20F-60 is significantly higher for SE-MSCs. This behavior is visible even more substantially in Figure 4c, which shows the areal capacitances of the two MSCs with 40 and 60 μm spacing at different scan rates. The main reason for the improved capacitive performance is the improved electrode thickness, as observed in Figure 3a. SE-20F-40 shows the highest C_A at 20 mV s^{-1} compared to C-

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ACS Omega 2020, 5, 5219−5228

20F-40 MSCs. The SE-20F-40 MSCs show a rate capability of 59.7%, while the C-MSCs exhibit a rate capability of 56.2%. Similarly, the energy density of the SE-MSC is 30.3 μJ cm^{-2}, higher than C-MSCs, 12.1 μJ cm^{-2}. At higher scan rates, the energy density for SE-20F-60 is 19.4 μJ cm^{-2} at 5000 mV/s. In contrast, the C-MSC could demonstrate an energy density of just 9.5 μJ cm^{-2}. The power density of the SE-MSCs for both 20F-40 and 20F-60 cases is better than that of C-MSCs. The highest power density achieved in the 20F-40 device was 96.9 μW cm^{-2} at 5000 mV/s, 1.9 times higher than the power density achieved with C-MSCs of the same configuration.

Volumetric capacitance, calculated from eq 3, provides a way of understanding the device when its performance is normalized by the volume of the electrode material. Because A is constant for the respective devices measured and C_t depends on the total charge stored in the activated GO electrodes, the total stored charge depends on the specific surface area (A_s) of the electrode. If A_s is the same for both C- and SE-MSCs, equivalent C_V values should be observed for the C- and SE-MSCs. Figure 4d displays the acquired volumetric capacitance of MSCs on C and SEsubstrates. The error bars are calculated by using the control deviation notations obtained from Figure 3b. In our current case, we see that all the devices have a volumetric capacitance of 0.90 ± 0.2 F cm^{-3}, which is in line with our stated assumption.

3.3. Discussion. The SE-MSCs have demonstrated a better capacitive behavior, higher energy density, and power density compared to the C-MSCs, as seen in Figures 4 and 5b. However, they still suffer from several issues that might make them incompatible with CMOS microelectronics at present. The EMIM-TFSI electrolyte is an ionic liquid, which can be ideally suitable for CMOS integration because of its high electrochemical window of 3 V. However, with both the SE- and C-MSCs, the operating window of the electrolyte was restricted to only slightly over 1 V. After 1 V, there was a clear indication of a stronger resistive behavior in the MSCs. The resistive trend was also observed at the cathodic interface while discharging. One of the reasons for a poor voltage window can be attributed to the splitting of water that is absorbed from the open environment during the measurement.[51] The issue of exposure to air is a consequence of the convenience required for carrying out multiple iterations of electrochemical characterization. This issue can be mitigated by encapsulation of the device with the electrolyte through glass or vacuum packaging. The CV measurements for SE-MSCs show another bump on the voltammogram at 1.25−1.35 V. This sudden increase in charge storage can be due to a reaction between the Fe layer and EMIM-TFSI ions and air;[52] adding such an active metal layer also results in a chemical reaction because in an open environment, water or oxygen in the air can be absorbed by the electrolyte solution and thence react with iron. Moreover, higher voltage makes reactions more active. The reaction is also visible during the discharging process.

A persistent issue with SE-MSCs is that they have a slightly worse rate capability because of substantial electrolyte resistance (R_{ct}), in line with Figures 4c and 5a. R_{ct} consists of the resistance of the electrolyte that depends on the geometric structure and electrolyte solution and contact resistance from the current collectors. The R_{ct} for the SE-MSCs was measured by investigating the intercept of the curves in Figure 5a on the Z_{real}-axis. For SE-MSC, the plot intersected the axis at 115 Ω, while the C-MSC demonstrated a value of 67 Ω. According to Conway et al.,[53] the slope of the Warburg impedance (I_W) provides an insight into the resistance observed at the pore interface of the electrode and electrolyte. An inspection of the slopes of curves in Figure 5a shows that the SE-MSCs exhibit a higher resistance at the pore interface of the electrode and electrolyte compared to the C-MSCs. A poor conductance in the Fe_a/Ti/Au current collectors due to higher surface roughness is likely to demonstrate such a result. All the above conclusions can be achieved through calibration of an equivalent circuit behavior shown in 5c. Table 1 shows the acquired values.

Table 1. List of Values of Parameters for SE- and C-MSCs Calculated from the Equivalent Circuit Model Shown in Figure 5c

circuit element	SE-MSC	C-MSC	units
R_{ct}	134.6	67.45	Ω
Y_o	5.6 μ	4.5 μ	S s
porosity	0.75	0.80	

Finally, after comparing the capacitance for SE- and C-MSCs over a range of input voltage frequencies in Figure 5b, it can be seen that the SE-MSCs show a stronger capacitive behavior until 524 Hz, while with C-MSCs, it is until 3.24 kHz. This is investigated by observing the frequency at which the SE and C curves start deviating from the straight line at lower frequencies. It is referred to as the knee-point. The knee-point marks the maximum frequency below which the supercapacitor shows a predominantly capacitive behavior.[54] Therefore, a high knee-point is generally preferred for MSCs. Furthermore, the SE-MSCs have poor capacitive performance at frequencies higher than its knee-point. This phenomenon can be attributed to the higher surface roughness of the SE-MSCs.[55] Increased roughness leads to a higher leakage current in capacitors.[56] This is the only trade-off for improving capacitance through surface roughening that cannot be addressed by performing further surface engineering.

In comparison to the devices produced in previous years,[57] the rGO-based MSCs fabricated through spin-coating do not perform as well as CVD-based devices. In some cases, the MSCs fabricated through the spin-coating technique in this paper demonstrate a power density of 96 μW cm^{-2}, significantly higher than the power densities of MSCs fabricated through ink-jet printing,[11,58−60] layer-by-layer method,[61] and electrophoretic deposition[62,63] of carbon-based electrodes. However, in several other cases, their performance is lower by 1 order of magnitude.[16] Rather than addressing the performance metrics of individual devices, the main purpose of using our approach of promoting surface roughness enhancement through annealed nanoparticles is to provide general means to improve the uniformity, adhesion, and coverage of the deposited solution, particularly by spin-coating. The approach can also be appropriated with spray-coating, ink-jet printing, and layer-by-layer deposition facilities or any technique which is at risk to suffer from poor surface adhesion of the electrode during lithography steps. We can improve the capacitive performance by increasing the number of spin-coated layers and viscosity of the solution, while utilizing the effects of the metal nanoparticle layer that would improve the wafer yield. The initial results for these tests can be found in the Supporting Information. Moreover, we can make channels for electrolytes as demonstrated by Li et al.[8] for packaged MSC devices for further integration with energy

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harvesters or sensors. Finally, as the fabrication process is CMOS-compatible, these devices can be easily integrated with either micro-energy harvesters or even the IC power management unit in a front-end-of-line of back-end-of-line configuration and can be utilized to charge temperature, pressure, or humidity sensors.[57]

4. CONCLUSIONS

MSCs fabricated through CMOS-compatible techniques such as spin-coating hold an enormous potential for realizing an integrated on-chip self-power unit for wireless sensors in the applications for Internet-of-things. In this paper, we have demonstrated that a substrate with an increased surface roughness due to a 4 nm annealed Fe layer enhances the performance of the MSCs fabricated through spin-coated GO electrode deposition. The electrode layers deposited on C and SE substrates demonstrate that the latter has a 78% increased thickness and a 21% improved mass retention. It also shows a 57% uniformity improvement of the electrode material coverage over a 2″ Si substrate. These improvements have led to gains in the performance of rGO-based MSCs in terms of areal capacitance, rate capability, energy density, and power density. Furthermore, a wafer yield of 87% was observed in the SE-MSC fabrication compared to only 33% in the C-MSCs. Most importantly, the devices positioned at the edge of the SE substrate demonstrated a near equivalent behavior to the devices at the center, thereby demonstrating an improved control on the performance of the devices fabricated on a single substrate. Although the SE-MSCs showed a higher R_E than the C-MSCs, perhaps due to the reactive nature of Fe with the electrolyte, the use of inert layers such as Ti, Pt, or Pd for nanoparticle formation can mitigate this challenge. Thus, utilization of surface enhancement techniques such as surface roughening can potentially enhance the performance of spin-coated MSCs, thereby making them a truly viable option for further on-chip integration with energy harvesters and electronics of wireless sensors, making them self-powered and with an extended or even infinite lifetime.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.9b04266.

Variation of GO spin-coating speeds and density and annealing temperatures (PDF)

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Notes

The authors declare no competing financial interest.

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