THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

MMIC-based Low Phase Noise Millimetre-wave Signal Source Design

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Abstract

Wireless technology for future communication systems has been continuously evolving to meet society's increasing demand on network capacity. The millimetre-wave frequency band has a large amount of bandwidth available, which is a key factor in enabling the capability of carrying higher data rates. However, a challenge with wideband systems is that the capacity of these systems is limited by the noise floor of the local oscillator (LO). The LO in today's communication systems is traditionally generated at low frequency and subsequently multiplied using frequency multipliers, leading to a significant degradation of the LO noise floor at millimetre-wave frequencies. For this reason, the thesis considers low phase noise millimetre-wave signal source design optimised for future wideband millimetre-wave communications.

In an oscillator, low frequency noise (LFN) is up-converted into phase noise around the microwave signal. Thus, aiming for low phase noise oscillator design, LFN characterisations and comparisons of several common III-V transistor technologies, e.g. GaAs-InGaP HBTs, GaAs pHEMTs, and GaN HEMTs, are carried out. It is shown that GaN HEMTs have good potential for oscillator applications where far-carrier phase noise performance is critical, e.g. wideband millimetre-wave communications.

Since GaN HEMT is identified as an attractive technology for low noise floor oscillator applications, an in-depth study of some factors which affects LFN characteristics of III-N GaN HEMTs such as surface passivation methods and variations in transistor geometry are also investigated. It is found that the best surface passivation and deposition method can improve the LFN level of GaN HEMT devices significantly, resulting in a lower oscillator phase noise.

Several MMIC GaN HEMT based oscillators including X-band Colpitts voltage-controlled-oscillators (VCOs) and Ka-band reflection type oscillators are demonstrated. It is verified that GaN HEMT based oscillators can reach a low noise floor. For instance, X-band GaN HEMT VCOs and a Ka-band GaN HEMT reflection type oscillator with 1 MHz phase noise performance of -135 dBc/Hz and -129 dBc/Hz, respectively, are demonstrated. These results are not only state-of-the-art for GaN HEMT oscillators, but also in-line with the best performance reported for GaAs-InGaP HBT based oscillators. Further, the MMIC oscillator designs are combined with accurate phase noise calculations based on a cyclostationary method and experimental LFN data. It has been seen that the measured and calculated phase noise agree well.

The final part of this thesis covers low phase noise millimetre-wave signal source design and a comparison of different architectures and technological approaches. Specifically, a fundamental frequency 220 GHz oscillator is designed in advanced 130 nm InP DHBT process and a D-band signal source is based on the Ka-band GaN HEMT oscillator presented above and followed by a SiGe BiCMOS MMIC including a sixtupler and an amplifier. The Ka-band GaN HEMT oscillator is used to reach the critical low noise floor. The 220 GHz signal source presents an output power around 5 dBm, phase noise of -110 dBc/Hz at 10 MHz offset and a dc-to-RF efficiency in excess of 10% which is the highest number reported in open literature for a fundamental frequency signal source beyond 200 GHz. The D-band signal source, on the other hand, presents an output power of 5 dBm and phase noise of -128 dBc/Hz at 10 MHz offset from a 135 GHz carrier signal. Commenting on the performance of these two different millimetre-wave signal sources, the GaN HEMT/SiGe HBT source presents the best normalized phase noise at 10 MHz, while the integrated InP HBT oscillator demonstrates significantly better conversion efficiency and still a decent phase noise.

Keywords: MMIC, phase noise, millimetre-wave, low frequency noise, D-band, InP DHBT, signal source, SiGe BiCMOS, GaN HEMT, VCO, passivation, frequency multiplier, deposition method.

List of publications

Appended publications

This thesis is based on the following papers.

[A] **T. N. T. Do**, M. Hörberg, S. Lai, D. Kuylenstierna, "Low Frequency Noise Measurements - A Technology Benchmark with Target on Oscillator Applications," in *44th European Microwave Conference (EuMC) Proceedings*, Oct. 2014, Rome, Italy, pp. 468-471.

[B] **T. N. T. Do**, A. Malmros, P. Gamarra, C. Lacam, M-A. Di Forte-Poisson, M. Tordjman, M. Hörberg, R. Aubry, N. Rorsman, D. Kuylenstierna, "Effects of Surface Passivation and Deposition Methods on the *1/f* Noise Performance of AlInN/AlN/GaN High Electron Mobility Transistors, " *IEEE Electron Device Letters,* vol. 36, no. 4, pp. 315-317, Apr. 2015.

[C] **T. N. T. Do**, S. Lai, M. Hörberg, H. Zirath, D. Kuylenstierna, "A MMIC GaN HEMT Voltage-Controlled-Oscillator with High Tuning Linearity and Low Phase Noise," in *2015 IEEE Compound Semiconductor Integrated Circuit Symposium*, 11-14 Oct. 2015, New Orleans, LA, USA, pp. 1-4.

[D] **T. N. T. Do**, M. Hörberg, S. Lai, S-H. Wollersjö, D. Johansson, H. Zirath, D. Kuylenstierna, "7-13 GHz MMIC GaN HEMT Voltage-Controlled-Oscillators (VCOs) for satellite applications," in *European Microwave Integrated Conference (EuMiC) Proceedings,* Oct. 2017, Nuremberg, Germany, pp. 220-223.

[E] **T. N. T. Do**, H. Zirath, D. Kuylenstierna, "220 GHz Oscillator in 130 nm InP HBT MMIC Technology," submitted to *IEEE Microwave Theory and Techniques (MTT)*, Sept. 2019.

[F] M. Bao, Z. S. He, **T. N. T. Do**, H. Zirath, "A 110-147 GHz Frequency Sixtupler in a 130 nm SiGe BiCMOS Technology," in *European Microwave Integrated Conference (EuMiC) Proceedings,* Oct. 2018, Marid, Spain, pp. 105-108.

[G] **T. N. T. Do**, M. Bao, Z. S. He, A. Hassona, D. Kuylenstierna, H. Zirath, "A low phase noise D-band signal source based on 130 nm SiGe BiCMOS and 0.15 μm AlGaN/GaN HEMT Technologies," in *International Journal of Microwave and Wireless Technologies,* vol. 11, special issue 5-6, Jun. 2019, pp. 456-465.

Other publications

[a] T. Hoang, O. Axelsson, **T. N. T. Do**, M. Thorsell, D. Kuylenstierna, N. Rorsman, "Influence on Noise Performance of GaN HEMTs With In Situ and Low-Pressure-Chemical_Vapor_Deposition SiN_x Passivation," *IEEE Transactions on Electron Devices*, vol. 63, no. 10, pp. 3887-3892, Aug. 2016.

[b] M. Hörberg, S. Lai, **T. N. T. Do**, D. Kuylenstierna, "Phase noise analysis of a tuned-input/tuned-output oscillator based on a GaN HEMT device," in *44th European Microwave Conference (EuMC) Proceedings*, 5-10 Oct. 2014, Rome, Italy, pp. 1118-1121.

[c] M. Hörberg, T. Emanuelsson, S. Lai, **T. N. T. Do**, H. Zirath, D. Kuylenstierna, "Phase Noise Analysis of an X-band Ultra-low Phase Noise GaN HEMT based Cavity Oscillator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 8, pp. 2619-2629, Aug. 2015.

[d] J. Stenarson, **T. N. T. Do**, H. Zhao, P. Sobis, A-Y. Tang, K. Yhland, J. Stake, "Sensitivity Analysis of TRL Calibration in Waveguide Integrated Membrane Circuits," *IEEE Terahertz Science and Technology*, vol. 3, no. 5, pp. 558-565, Aug. 2013.

[e] H. Zhao, **T. N. T. Do**, P. Sobis, A-Y. Tang, K. Yhland, J. Stenarson, J. Stake, "Characterization of thin film resistors and capacitors integrated on GaAs membranes for submillimeter wave circuit applications," in *23rd International Conference on Indium Phosphide and Related Materials*, Berlin, Germany, May. 2011, pp. 1-4.

[f] J. Stenarson, K. Yhland, **T. N. T. Do**, H. Zhao, P. Sobis, J. Stake, "Influence of waveguide width errors on TRL and LRL calibrations," in *79th Microwave Measurement Conference (ARFTG)*, Montreal, Quebec, Jun. 2012, pp.1-3.

Thesis

[g] **T. N. T. Do**, "GaN HEMT Low Frequency Noise Characterization for Low Phase Noise Oscillator Design," Licentiate dissertation, Dept. of Microtechnology and Nanoscience. Dept. Microtechnology and Nanoscience, Chalmers University of Technology, Sweden, Dec. 2015.

As a part of the author's doctoral studies, some of the work has previously been published in [g]. Text, figures and tables from [g] may therefore be fully or partly reproduced in this thesis.

Notations and abbreviations

Notations

A_b	Fitting parameter in *G-R* noise model
A_f	Fitting parameter in *1/f* noise model
$\alpha(\omega_0 t)$	Normalized periodic function
α_H	Hooge parameter
C	Capacitance
C_j	Bias dependence capacitance of varactor
C_{max}	Maximum capacitance of varactor
C_{min}	Minimum capacitance of varactor
C_0	Zero bias capacitance
C_p	Parallel capacitance of parallel resonator
C_s	Serial capacitance of serial resonator
c_0	DC value of impulse sensitive function
c_n	Real valued coefficients of impulse sensitive function
Δf	Noise bandwidth
$\Delta\omega$	Small displacement from the angular oscillation frequency ω
f_{1/f^3}	$1/f^3$ corner frequency
F	Fitting parameter
f	Frequency
f_b	Frequency where *G-R* centers are activated
F_{fe}	Fitting parameter in *1/f* noise model
f_m	Offset frequency
f_{max}	Maximum oscillation frequency
f_T	Current-gain cut-off frequency
f_0	Oscillation frequency
ϕ_n	Phase noise
$i_n(t)$	Cyclostationary noise source
$i_{n0}(t)$	Stationary noise source
k	Boltzmann's constant
K_b	Fitting parameter in *G-R* noise model
K_f	Fitting parameter in *1/f* noise model
L	Inductance
L_p	Parallel inductance of parallel resonator
L_s	Serial inductance of serial resonator
$\mathcal{L}(f_m)$	Single sideband phase noise at offset frequency f_m
n	Colpitts capacitance division ratio
N	Number of carriers
η	Factor depending on the doping profile in p-n junction

q	Electron charge
q_{max}	Maximum charge stored in the tank
Q_0	Unloaded quality factor
Q_{ext}	External Q-factor
Q_L	Loaded quality factor
R	Resistance
R_p	Parallel resistance of parallel resonator
R_s	Serial resistance of serial resonator
S_G	Conductance noise spectrum
S_I	Current noise spectrum
S_R	Resistance noise spectrum
S_V	Voltage noise spectrum
Γ	Impulse sensitive function
Γ_{eff}	Effective impulse sensitive function
Γ_{rms}	RMS value of impulse sensitive function
T	Temperature
T_p	Power transmission loss ratio at resonance
V_{bb}	Base bias
V_{cc}	Collector bias
V_{dd}	Drain bias
V_{gg}	Gate bias
V_v	Varactor voltage
ω	Angular frequency
Ψ_0	Built-in potential of p-n junction
P_{DC}	DC power consumption
P_{out}	Output power
Z	Impedance
Z_0	Characteristic impedance

Abbreviations

ALD	Atomic Layer Deposition
AlGaN	Aluminum Gallium Nitride
AlInN	Aluminum Indium Nitride
Al_2O_3	Aluminum Oxide
AM	Amplitude Modulation
BiCMOS	Bipolar Junction transistor and Complementary metal-oxide-semiconductor
DC	Direct Current
DSA	Dynamic Signal Analyzer
DUT	Device Under Test
EM	Electromagnetic
FET	Field Effect Transistor
FFO	Fixed Frequency Oscillator
FFT	Fast Fourier transform
FOM	Figure of Merit
FOM_T	Figure of Merit of tunable oscillators
GaN	Gallium Nitride
GaAs	Gallium Arsenide
G-R noise	Generation Recombination noise
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
InGaP	Indium Gallium Phosphide
ISF	Impulse Sensitivity Function
InP	Indium Phosphide
LFN	Low Frequency Noise
LTI	Linear Time Invariant
LTV	Linear Time Variant
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
PECVD	Plasma Enhanced Chemical Vapor Deposition
pHEMT	Pseudomorphic High Electron Mobility Transistor
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
SiGe	Silicon Germanium
SiN	Silicon Nitride
SNR	Signal to Noise Ratio
VCO	Voltage Controlled Oscillator

Contents

Chapter 1

Introduction

1.1 The evolution of wireless communication systems

Since the very early stage of human society, the demand on communication to exchange information with each other has been considerable. Communication is described in many different forms such as spoken, written words, tone of voice or smoke signals, etc. [1]. Together with the evolution of society, the technology for communication has been gradually developed. In 1831, the first telegraph was invented by Joseph Henry [2]. Some years later, Samuel Morse invented the Morse code [3]. In 1876, the first telephone was invented by Alexander Graham Bell [4]. In 1896, Guglielmo Marconi demonstrated the first wireless transmission in which Morse code signals were transmitted a distance of 3.2 km using radio frequency (RF) electromagnetic waves [5]. Marconi's invention of wireless transmission defines a milestone in communication technology in which the signal is carried by electromagnetic waves over very long distances without wires or cables, leading to the evolution of today's wireless communications, e.g. mobile communication, Wi-Fi, Bluetooth, etc. Among these applications, mobile wireless communication brought a revolution on the way people communicate. The first generation of mobile communication (1G) was utilised in early 1980s using analog signal technology. Only voice was supported in 1G with limited capacity. The second generation of mobile communication (2G) was deployed in 1991 using digital signal technology, enabling not only voice but also short message service (SMS) with better quality of service. The third generation of mobile communication (3G) was introduced in 2000 which offers voice, SMS as well as multimedia services such as video conference with higher speed. 3G also marked a turning point/transition from regular phone to smartphone. After the introduction of 3G, smartphones became popular around the world. The huge demand on data usage in smartphones leads to the need for the fourth generation of mobile communication (4G) which supports a higher data rate and more advanced multimedia services such as multimedia messaging service (MMS), high quality streaming video, etc. Today, 4G is spread around the world, but the data traffic demand still keeps increasing dramatically over years [6-7]. Fig. 1-1 shows the evolution of data rates in technologies for mobile cellular over decades [8-16]. This demand pushes the future wireless communication systems towards new innovations to further increase network capacity. The fifth generation of mobile communication (5G) starts to be

prepared to hit the market by 2020. 5G is expected to offer data rates up to 10 gigabits per second (Gbps) for an individual user, higher efficiency and higher reliability multimedia services [16], which comes with new challenges for technology for the mobile access network as well as mobile backhaul network. To handle the demands on capacity in the wireless mobile networks, increasingly higher frequencies and larger bandwidths are used.

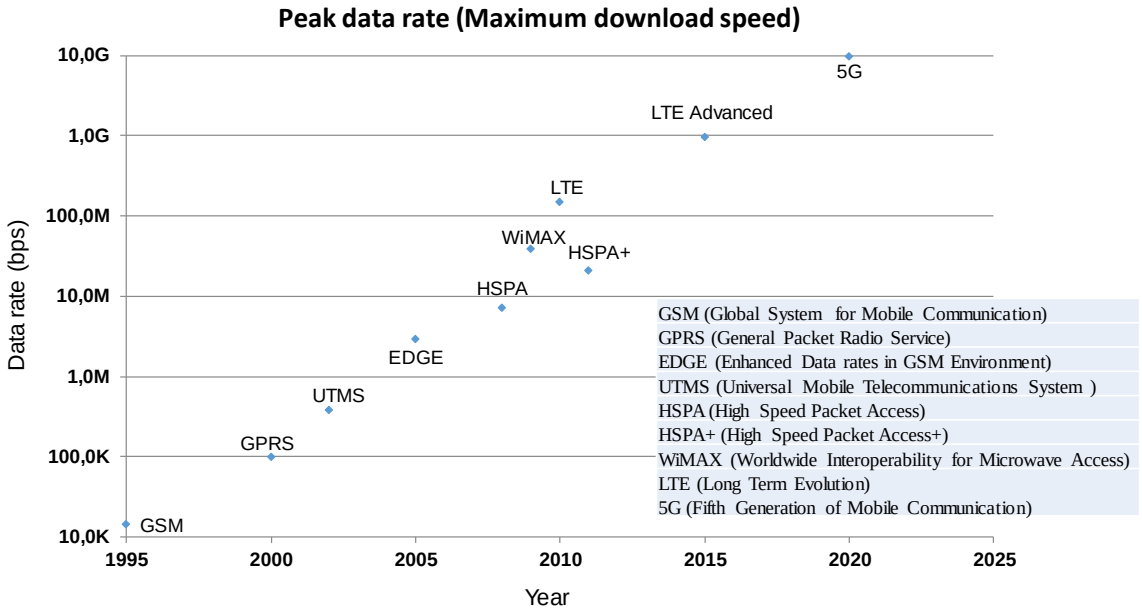


Fig. 1-1. The evolution of data rates in mobile cellular technologies over decades. The peak data rate is the theoretical data rate for each technology assuming a low motion, perfect coverage and no congestion [8-16].

1.2 Design considerations for future wireless communication systems

As mentioned above, the future wireless communication systems, e.g. 5G, need to support higher speed and capacity. According to Claude Shannon, the capacity of a single communication channel may be increased by either larger bandwidth or improved spectral efficiency [17]. The spectral efficiency that can be achieved is further limited by the signal to noise ratio (SNR) of the communication channel. Conventional frequency bands used today, e.g. up to 86 GHz for microwave backhaul, already address relatively advanced modulation formats and can be considered to be limited by bandwidth [18]. Naturally, the most promising pathway to increasing data rates in future telecommunication systems is exploring the large absolute bandwidth available at millimetre-wave frequencies (up to 300 GHz). It has been reported that the future frequency bands used for microwave backhaul will be moved beyond 100 GHz to open more spectrum [19]. It can be seen that future wireless communication systems need to support simultaneously large bandwidth and high order modulations to meet increasing

demands of data rates.

However, moving to the millimetre-wave band presents challenges in hardware design, for instance in the frequency generation. In recent years, several high-data rate communication tests, deploying wideband signals beyond 100 GHz, have been demonstrated [20-24]. However, still none of these experiments have demonstrated simultaneously large bandwidth and high spectral efficiency. It has been experimentally demonstrated that the capacity of wideband systems might be limited by the level of local oscillator (LO) noise floor [25]. Thus, new architecture for low noise floor signal source design optimised for wideband millimetre-wave communication to enable higher data rates is necessary.

To reach a low noise floor, the LO signal can be generated at fundamental millimetre-wave frequency instead of being generated at relatively low frequency and then subsequently multiplied by frequency multiplier which is common method in current systems. Millimetre-wave signal sources operating beyond 100 GHz can be implemented in advanced Si and III-V semiconductor processes. So far, advanced 130 nm SiGe BiCMOS HBTs and 130 nm InP DHBTs with a maximum oscillation frequency (f_{max}) up to 500 GHz and 1 THz, respectively, have been reported [26-27]. However, the performance of signal source tends to degrade when the frequency increases due to degradation of quality (Q) - factor of the resonator and the output power of oscillators at high frequencies. Most of the fundamental frequency millimetre-wave signal sources reported in Si and III-V technologies have low output power [28-34].

On the other hand, a low noise floor can be reached with a high SNR. Therefore, a technology with high output power is beneficial. Consequently, short gate length AlGaN/GaN high electron mobility transistor (HEMT) technology is a potential candidate for low phase noise millimetre-wave frequency generation thanks to its high breakdown voltage. It has been demonstrated that fundamental GaN HEMT based oscillators are able to achieve high output power with low far-carrier phase noise (low noise floor) [35-37]. However, GaN HEMT MMIC process for the implementation of fundamental GaN HEMT based signal source above 100 GHz are rarely available. Further, III-V technologies, such as AlGaN/GaN HEMT, cannot compete with the integration levels of CMOS and BiCMOS technology. A silicon technology will most likely be needed for the clock-recovery. Recently, good frequency multipliers and mixers have been demonstrated in SiGe HBT technology [38-39]. In this perspective, a combination of AlGaN/GaN HEMT and BiCMOS technologies is a promising candidate for future high-end millimetre-wave wideband communication systems. For example, the signal can be generated at an intermediate high frequency by GaN HEMT oscillator to reach low noise floor and followed by a state-of-the-art frequency multiplier implemented in SiGe BiCMOS technology with low multiplication factor to millimetre-wave bands [40].

Besides, it is known that the phase noise of a signal source is affected by low frequency noise (LFN) of active device. Thus, the LFN characterisation and methods to improve LFN characteristic of a transistor, e.g. different passivation methods, are other important aspects to investigate for low phase noise signal source design [41-43].

1.3 Thesis contributions and outline

This thesis reports on techniques for design of low phase noise MMIC signal sources at millimetre-wave frequencies.

Since the phase noise of an oscillator (signal source) is affected significantly by the LFN level in active device, the LFN of common III-V transistor technologies, i.e. GaN HEMTs, GaAs pHEMTs, GaAs InGaP HBTs are characterised and compared for the design of low phase noise signal sources in paper [A]. Paper [A] has shown that GaN HEMT is a good candidate for low phase noise oscillator design in which the low noise floor is crucial, e.g. in wideband millimetre-wave wireless communications.

Since GaN HEMT is attractive technology for low noise floor oscillator design, paper [B] investigates further on some factors which affect LFN of GaN HEMT devices. It has been shown in paper [B] that the surface passivation and deposition methods have major impact on the LFN level of GaN devices which can lead to a big improvement on the phase noise in an oscillator design (assuming that the oscillator is well designed).

The implementation of low phase noise MMIC GaN HEMT based oscillators including X-band GaN HEMT voltage-controlled-oscillators (VCOs) and Ka-band GaN HEMT reflection type oscillator are presented in papers [C], [D] and [G], respectively. It is found that the 1 MHz phase noise performance of the presented GaN HEMT based oscillators are state-of-the-art, e.g. -135 dBc/Hz for X-band GaN HEMT VCOs and -129 dBC/Hz for the Ka-band GaN HEMT oscillator and slightly better than the state-of-the-art GaAs InGaP HBT oscillators which have been usually used in traditional communication systems. The results in papers [C], [D] and [G] are consistent with the conclusion in paper [A] that GaN HEMT based oscillators can reach a low noise floor.

Then, two architectures for low phase noise millimetre-wave signal source designs are realised, i.e. low phase noise fundamental millimetre-wave signal source and low phase noise fundamental intermediate frequency signal source multiplied to millimetre-wave by frequency multiplier. The signal source in the first architecture presented in paper [E] is designed at fundamental 220 GHz based on advanced InP DHBT process. This signal source has state-of-the-art results in term of power (5 dBm), phase noise at 10 MHz offset (-110 dBc/Hz) and dc-to-RF efficiency (12%) for a millimetre-wave signal source beyond 200 GHz. For the second architecture, the frequency multiplier is needed and the sixtupler implemented in SiGe BiCMOS process with state-of-the-art result is shown in paper [F]. Paper [G] demonstrates a D-band signal source in the latter architecture by combining the presented low phase noise Ka-band GaN HEMT reflection type oscillator and MMIC SiGe circuit consisting of the sixtupler presented in paper [F] and an amplifier. The 10 MHz phase noise performance of this signal source is -128 dBc/Hz which is the lowest number reported for a D-band signal source. In addition, the circuit designs in papers [C], [D], and [E] are combined with the phase noise calculation based on time-invariant method and a good agreement is reached for the measured and calculated phase noise.

The thesis is arranged as follows. Chapter 2 gives details on technologies used in the circuit design of this thesis, i.e. InP DHBTs, GaN HEMTs, SiGe BiCMOS. Chapter 3 presents general considerations for low phase noise signal source design such as noise origins, the resonator, phase noise, phase noise models, varactor, oscillator specification and figures of merit. Then, Chapter 4 presents LFN characterisation including LFN setups,

the comparison on LFN measurements of different III-V transistor technologies such as InGaP HBT, GaAs pHEMT, and GaN HEMT and the studies on GaN HEMT LFN characteristic. Varactor characterisation, the methodologies for phase noise measurement, flicker noise modeling and accurate phase noise calculation are also discussed in Chapter 4. Chapter 5 presents low phase noise MMIC GaN HEMT based signal source design and two low phase noise millimetre-wave signal source designs based on two different architectures. The first architecture generates the signal at fundamental high frequency based on an advanced InP DHBT process. The latter architecture combines low phase noise GaN HEMT signal source generated at fundamental intermediate frequency and SiGe BiCMOS frequency multiplier to frequency multiply the signal to millimetre-wave band. Finally, Chapter 6 presents the conclusions from this work.

Chapter 2

Semiconductor technologies used in this thesis

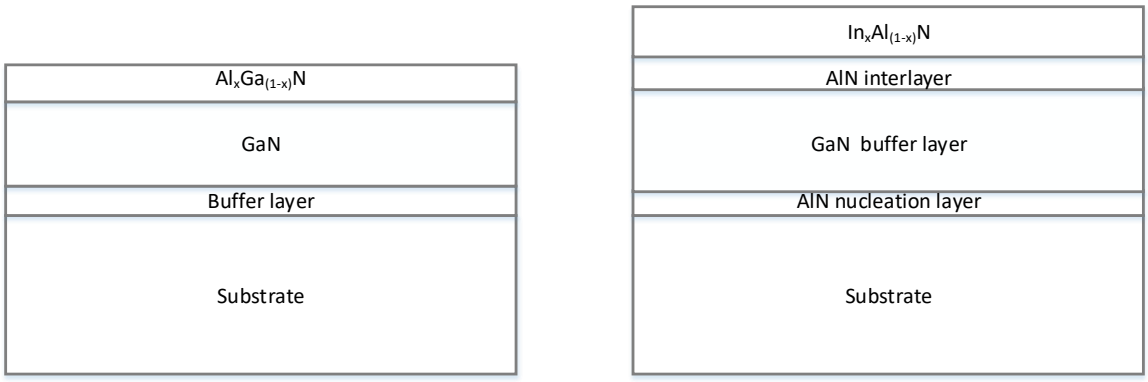
Semiconductors have made a big change to the world and nowadays they appear in most electric and electronic appliances in everyday life. In the latter half of 20th century, many semiconductor materials were explored. Among of them, silicon is the most common material used in commercial appliances due to its low cost, high yield and relatively high thermal conductivity. It is the most important element in monolithic integrated circuits (ICs) and computer chips. Besides, its compounds, i.e. alloying silicon with other materials, also play an important role in semiconductor industry. For examples, silicon germanium (SiGe) is widely used in high speed heterojunction bipolar transistors [44]; and silicon carbide (SiC) is employed in detectors, etc. After Si, gallium arsenide (GaAs) is the second most commonly used semiconductor which is widely used in ICs, diodes, solar cells, and so on. Recently, indium phosphide (InP) and gallium nitride (GaN) become materials for high speed heterojunction bipolar transistors (HTBs) and high electron mobility transistors (HEMTs), respectively, in millimetre-wave and sub millimetre-wave applications. So far, state-of-the-art performance in terms of cut off frequency (f_T) and maximum oscillation frequencies (f_{max}) for both InP-based HBTs and GaN-based HEMTs have been reported. For examples, f_{max} up to 1.1 THz and 444 GHz have been shown for advanced 130 nm InP DHBT and 20 nm GaN HEMT [27, 45].

The circuit design in this thesis work bases on three different semiconductor technologies, i.e. GaN HEMT, InP DHBT and SiGe BiCMOS.

2.1 GaN HEMT technology

GaN is a promising material for high power and high frequency applications thanks to its very wide bandgap property and high saturation electron velocity. In general, two types of GaN-based HEMT are developed: the traditional AlGaN/GaN HEMT and the alternative AlInN/AlN/GaN HEMT [46-48]. The AlGaN/GaN HEMT process is already commercialised while InAlN/AlN/GaN HEMT technology is on research level. The motivation of using Indium (In) in AlInN/AlN/GaN is to reach higher f_T/f_{max} compared to the conventional AlGaN/GaN HEMT [48]. Essentially, a GaN-based HEMT is grown on

SiC substrate. For AlGaN/GaN HEMT, the layer structure typically consists of a buffer layer, an undoped GaN layer and a barrier layer AlGaN [46] while the heterostructure of AlInN/AlN/GaN HEMT comprises an AlN nucleation layer, a GaN buffer, an intermediate AlN layer and an AlInN layer [48]. Fig. 2-1 shows the layer structure of two types of GaN-based HEMT. In this work, both GaN HEMT types are used. The commercial AlGaN/GaN HEMTs are fabricated by different vendors, e.g. United Monolithic Semiconductors (UMS) Technologies, France and Qorvo Technologies, USA, while AlInN/AlN/GaN HEMT devices are fabricated by Chalmers MMIC process. The 0.25 µm AlGaN/GaN HEMT UMS's process and 0.15µm AlGaN/GaN HEMT Qorvo's process have f_T of 30 GHz and 53 GHz, respectively, while AlInN/AlN/GaN HEMT from Chalmers MMIC process has 180 nm gate length with f_T /f_{max} of 47/100 GHz.



(a) (b)

Fig. 2-1. The layer structure of two types of GaN-based HEMT. (a) AlGaN/GaN HEMT. (b) AlInN/AlN/GaN HEMT.

2.2 InP DHBT technology

InP is attractive for high power and high frequency electronics thanks to its superior electron velocity and relatively large breakdown voltage. Both InP-based DHBT and InP-based HEMT are identified as potential candidates for millimetre wave applications [49-50]. This thesis work covers results based on the advanced 130 nm InP DHBT processes developed by Teledyne Technologies, USA [51]. Fig. 2-2 shows cross-section of the 130 nm InP DHBT process. This process has 3 metal layers (MET1 – MET3) with the possibility of using either MET1 or MET3 as ground plane, metal-insulator-metal (MIM) capacitors and thin film resistors (TFRs). Between metal layers, a benzocyclobutene (BCB) (dielectric of 2.7) with different spacings, i.e. 1 µm between MET1 and MET2 and 5 µm between MET2 and MET3, is utilised as interlayer dielectric. MET2 and MET3 layers have the same thickness of 1 µm while MET1 has a thickness of 0.6 µm. This process has f_T of >520 GHz and f_{max} exceeding 1.1 THz.

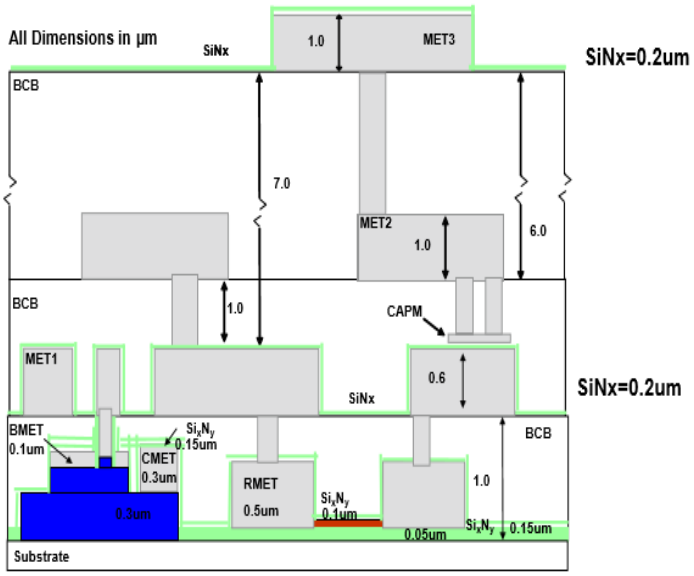


Fig. 2-2. Representative cross-section of 130 nm InP DHBT IC technology (from Teledyne Technologies).

2.3 SiGe BiCMOS technology

SiGe BiCMOS HBTs are widely used in applications such as automotive radar, high-speed wireless communications, etc., thanks to its unique capability to combine superior properties of SiGe material, i.e. high speed and relatively high breakdown voltage compared to Si and advanced high integration level of CMOS [44]. SiGe BiCMOS technology enables Si-based RF system on chip solution with high f_T and f_{max} which is out of reach with existing integrated Si-based HBT technology and therefore is competitive for high speed, high frequency and low power electronic applications.

The SiGe BiCMOS technology used in this thesis is developed by Infineon Technologies with 130 nm gate length [52]. Fig. 2-3 shows the cross-section of 130nm SiGe BiCMOS process. In this process, there are 6-metal layers with 4 thin lower layers (M1 to M4) and 2 thick upper layers (M5-M6). MIM capacitors are realised between M5 and M6 while M4 is usually chosen as ground plane. This process also enables two types of resistors, namely metal film resistor with low resistivity and poly resistor with high resistivity. There are 3 types of npn transistors in this process, i.e. high-speed transistors, medium-speed transistors and high-voltage transistors, offering the f_T of 250 GHz, 100 GHz and 50 GHz, respectively, for common-emitter configuration.

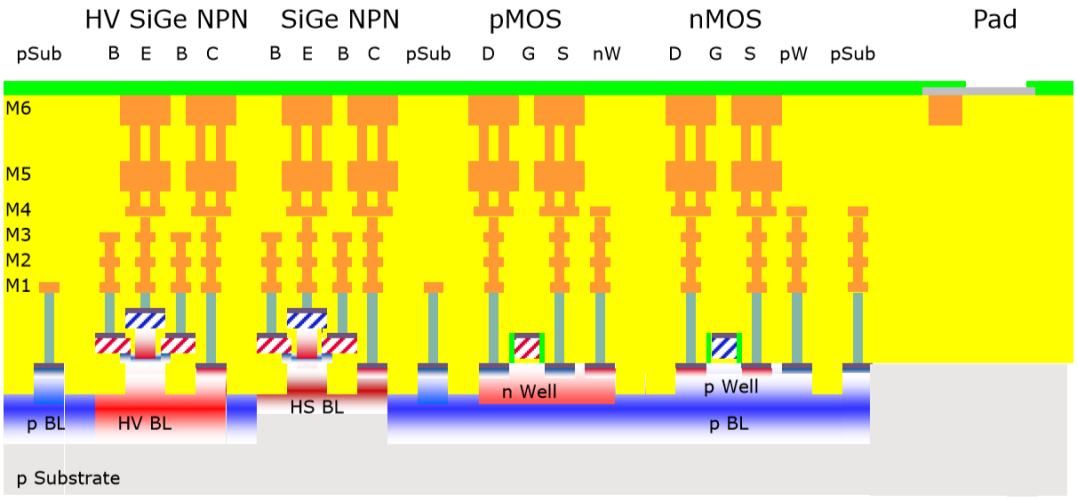


Fig. 2-3. Representative cross-section of 130 nm SiGe BiCMOS IC technology (from Infineon Technologies).

Chapter 3

Challenges in low phase noise signal source design

This chapter presents challenges in low phase noise signal source design. The noise sources that influence the oscillator's phase noise are introduced in section 3.1. Section 3.2 presents fundamentals of phase noise in oscillators including the oscillator representation, the resonator, the definition of phase noise, phase noise models. The varactor that determines frequency tuning in voltage-controlled-oscillator (VCO) design is described in section 3.3. Section 3.4 presents the oscillator specification and figures of merit.

3.1 Noise sources

3.1.1 Thermal noise

Thermal noise is produced by the random thermal motion of electrons [53]. It was formulated the first time by Johnson and Nyquist in 1926, so it is usually referred as Johnson-Nyquist noise. Thermal noise is directly related to the absolute temperature T and is not affected by the applied voltage or current. In a resistor, thermal noise is a white Gaussian noise. Thermal noise can be modeled by a series voltage generator or a shunt current generator as

$$\overline{v^2} = 4kTR\Delta f$$
$$\text{or } \overline{i^2} = 4kT\frac{1}{R}\Delta f \qquad (3\text{-}1)$$

where k is Boltzmann's constant, R is the circuit resistance, Δf is the bandwidth in Hertz and T is the absolute temperature. At room temperature (300°K), $4kT \approx 1.66 \cdot 10^{-20}$ V-C.

3.1.2 Shot noise

Shot noise is related to current fluctuations caused by carriers travelling across the potential barrier at the junction of a diode. Consequently, it is also present in bipolar junction transistors (BJTs), e.g. at the base-collector and the base-emitter junctions [53]. Shot noise in field effect transistors (FETs) is related to the DC gate current which can usually be neglected. In similar to thermal noise, shot noise has a white distribution in frequency domain but is manifested by a discrete nature represented by a Poisson distribution. The level of the shot noise may be modelled as

$$\overline{i^2} = 2qI_D\Delta f \tag{3-2}$$

where $q = 1.6\times10^{-19}$ C is the electron charge, I_D is the bias current.

3.1.3 Flicker noise

Flicker noise is found in all active devices. It is also called *1/f* noise since the noise amplitude is inversely proportional to the frequency [54]. Similar as other types of noise, flicker noise can be expressed in form of resistance noise spectrum (S_R), voltage noise spectrum (S_V), current noise spectrum (S_I) or conductance noise spectrum (S_G), and the spectra are usually normalized, e.g. S_R/R^2, S_V/V^2, S_I/I^2 *or* S_G/G^2. In 1969, Hooge proposed that the fluctuations in conductivity cause *1/f* noise [55]. The conductivity fluctuations lead to changes in the resistance. Since the resistance varies with number of carriers and the carrier mobility, changes in one of the two terms generate *1/f* noise. This leads to two major *1/f* noise models: one based on the fluctuations in carrier density and the other based on the mobility fluctuations. Also in [55], an empirical relation was proposed by Hooge in which *1/f* noise is inversely proportional to the number of carriers in the device.

$$\frac{S_R}{R^2} = \frac{\alpha_H}{N\cdot f} \tag{3-3}$$

where N is the number of carriers in the device, f is the frequency and α_H is the Hooge parameter.

According to Hooge, α_H depends on the crystal quality and scattering mechanisms. He also proposed an average Hooge parameter of 2×10^{-3} and this value could be 2 or 3 orders of magnitudes lower in a good material. The Hooge parameter has been used as figure of merit for characterising *1/f* noise of many materials and devices [43, 56-59]. However, most of LFN characterisations in open literature were often taken at low voltage biases which are not applicable for most of circuit applications. C. Sanabria claims that Hooge parameter should be used only for material comparisons, not for device comparisons [54].

The exact origin of flicker noise is unclear; however, it is mainly associated with traps and defects in the device. The traps capture and release carriers randomly, leading to noise increase with energy concentrated at low frequencies. Flicker noise has a large impact on integrated circuits, especially on oscillators. In general, the level of flicker noise is much

lower in BJTs compared to FETs.

Flicker noise is usually modeled as [60]

$$\overline{i^2} = K_f \frac{I_{DC}^{A_f}}{f^{F_{fe}}} \Delta f \tag{3-4}$$

where K_f, A_f, and F_{fe} are fitting parameters, respectively, describing the noise level, the noise current dependency, and the noise frequency dependency.

3.1.4 Generation-Recombination noise

Generation- Recombination (G-R) noise is generated by fluctuations in the number of free charge carriers in semiconductor materials related to the random transitions of carriers between different energy bands, e.g. between conduction and valence bands, etc. [61]. *G-R* noise has Lorentzian power spectral density which is expressed as [55]

$$\frac{S_R}{R^2} = \frac{S_G}{G^2} = \frac{S_N}{N^2} = \frac{\overline{(\Delta N)^2}}{N^2} \cdot \frac{4\tau}{1+\omega^2\tau^2} \tag{3-5}$$

where τ is a relaxation time which is a characteristic of the trap, ω is the angular frequency, $\overline{(\Delta N)^2} / N^2$ is the fluctuation quantity.

G-R type of noise current can be modeled as [60]

$$\overline{i^2} = K_b \frac{I_{DC}^{Ab}}{1+\left(\frac{f}{f_b}\right)^2} \Delta f \tag{3-6}$$

where K_b and A_b are fitting parameters, f_b is the frequency when G-R centers are activated. G-R noise has Lorentzian's frequency shape.

3.2 Fundamentals of phase noise in oscillators

3.2.1 Oscillator representation

An oscillator is an electronic circuit which can generate a periodic signal (voltage, current) by converting DC power to RF power. The oscillator is one of the key building blocks in many digital electronic and RF communication systems. There are commonly used methods for analysis of oscillators: the feedback oscillator and negative resistance oscillator approaches [62]. In the feedback approach, the oscillator is considered as an amplifier with a positive feedback network as shown in Fig. 3-1. The amplifier and the

feedback will form a loop and the condition for oscillation is that a part of output signal is combined in phase with the input signal and the amplitude of the loop gain is larger than 1, as expressed in equations (3-7) to (3-9).

$$V_{out}(s) = V_{in}(s) \cdot \frac{A(s)}{1 - A(s)B(s)} \tag{3-7}$$

$$\left|A(s)B(s)\right| > 1 \tag{3-8}$$

$$\angle A(s)B(s) = n2\pi \tag{3-9}$$

where *A(s)*, *B(s)* are the gains and $\angle A(s), \angle B(s)$ are the phases of the amplifier and the feedback network, respectively.

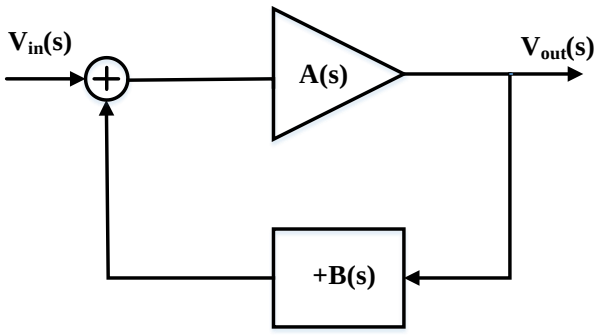


Fig. 3-1 Block diagram of a feedback oscillator.

Fig. 3-2 displays a block-level schematic for a negative resistance oscillator. It has a passive resonator separated from the amplifying active element. Each side is considered as a one-port network. The oscillation condition may be expressed by the reflection coefficients. The oscillation occurs when reflection coefficients of the two sides are in phase and their amplitudes' product is greater than unity, which may be expressed

$$\left|\Gamma_R(s)\Gamma_A(s)\right| > 1 \tag{3-10}$$

$$\angle \Gamma_R(s)\Gamma_A(s) = n2\pi \tag{3-11}$$

where $\Gamma_R(s)$ and $\Gamma_A(s)$ are the reflection coefficients of the passive resonator and the amplifying active element, respectively.

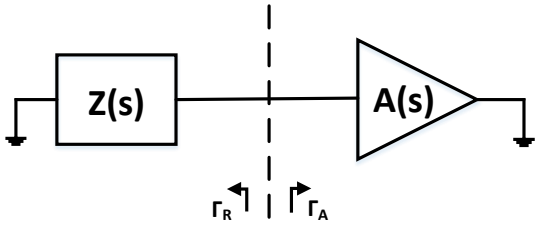


Fig. 3-2 Block diagram of a negative resistance oscillator.

3.2.2 Resonator

The loss of a passive resonator is often characterised by a quality factor (*Q*-factor). The *Q*-factor is expressed by the ratio between stored energy and average dissipated power, i.e. power loss,

$$Q = \omega \times \frac{E_{stored}}{P_{diss}} \tag{3-12}$$

The general definition of *Q*-factor in (3-12) is often not the most efficient for measurement extraction. Circuit theory shows that the *Q*-factor may also be extracted from the frequency-to-bandwidth ratio of the resonator or the phase-frequency slope of the resonator input impedance. The first one is performed as

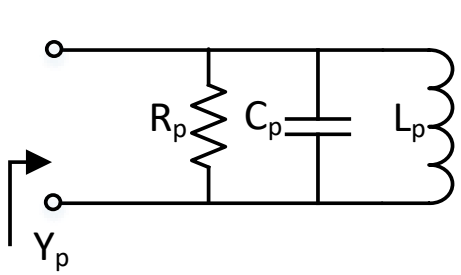
$$Q = \frac{\omega_0}{\Delta\omega_{3dB}} \tag{3-13}$$

where ω_0 is the resonance frequency and $\Delta\omega_{3dB}$ is the 3-dB resonator bandwidth.

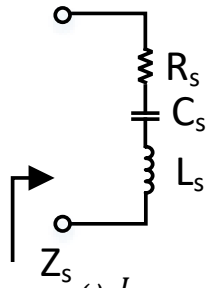
The latter one is the phase slope of the input impedance Z. For a parallel/serial resonator, the *Q*-factor can be expressed by

$$Q = \mp \frac{\omega_0}{2} \frac{d\phi(Z_{p/s})}{d\omega}\bigg|_{\omega=\omega_0} \tag{3-14}$$

If lumped components are used, the *Q*-factor can be calculated directly from the component values, as seen in in seen in Fig. 3-3 and expressed in (3-15) to (3-16).



(a) $Q = \frac{R_p}{\omega_0 L_p} = \omega_0 C_p R_p$ (3-15)



(b) $Q = \frac{\omega_0 L_s}{R_s} = \frac{1}{\omega_0 C_s R_s}$ (3-16)

Fig. 3-3. Schematic of parallel resonance circuit (a) and serial resonance circuit (b).

The *Q*-factor of the resonator is critical for integrated oscillators design. A high *Q*-factor (low loss) resonator is usually desired. However, most monolithic microwave integrated circuit (MMIC) components have relative low *Q*-factor.

When the resonators are not connected to the load, the characterised Q-factor is called unloaded *Q*-factor, Q_0. On the other hand, in practice the resonator always needs to connect with the active element which injects energy into it. In other words, it will always

be loaded by its internal load. This load network is characterised by an external *Q*-factor, Q_{ext} and the total loaded *Q*-factor, Q_L, can be calculated as

$$\frac{1}{Q_L} = \frac{1}{Q_0} + \frac{1}{Q_{ext}} \tag{3-17}$$

3.2.3 Phase noise

An ideal output signal generated from an oscillator is a pure sinusoid at a single frequency. It can be described in time domain as

$$V(t) = A_0 \sin\left(2\pi f_0 t\right) \tag{3-18}$$

where A_0 is the nominal amplitude and f_0 is the nominal frequency.

In frequency domain, the ideal signal is shown as an impulse function at single frequency. However, in practice, an electronic signal always has small random fluctuations in amplitude and phase which are known as amplitude and phase noise. These have their origin in LFN that is up-converted around the microwave carrier, Fig. 3-4. Phase noise in frequency domain can be equivalently described by jitter in time domain. The real signal can be expressed as

$$V(t) = \left[A_0 + A_n(t)\right]\sin\left(2\pi f_0 t + \Phi_n(t)\right) \tag{3-19}$$

where A_n(t) is amplitude noise and Φ_n(t) is phase noise.

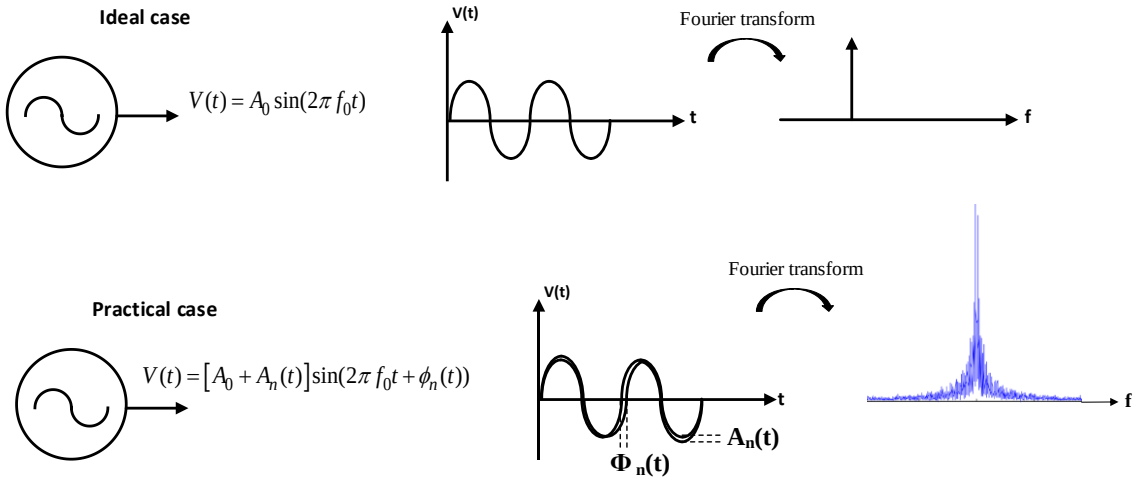


Fig. 3-4. A sinusoidal signal generated from an oscillator in the ideal case and the practical case (with phase and amplitude noise).

In wireless communication systems and radar systems, phase noise is one of the most interesting and important characteristics. It has been shown that the phase noise of VCOs in the systems using advanced modulation techniques, e.g. 1024 QAM, is one of the main limiting factors of system performance [63]. Compared to phase noise, amplitude noise is

less important since its effect is usually suppressed when the active device goes into compression.

3.2.4 Phase noise models

An early phase noise model was proposed by D. B. Leeson in 1966 [64]. Assuming that the circuit has only thermal noise, the single sideband phase noise in *1/f²* region is expressed as

$$\mathcal{L}(f_m) = 10\log_{10}\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{f_0}{2Q_L f_m}\right)^2\right]\right\} \tag{3-20}$$

where f_0 is the output frequency, f_m is the offset from the oscillation frequency, F is a fitting parameter, k is Boltzmann's constant, Q_L is the loaded quality factor, P_s is the power swing over the resonator.

In reality, the active device is also affected by flicker noise. When two noise components are mixed at low frequencies, Leeson has given an empirical equation of single sideband phase noise which includes the effect of flicker noise up-conversion as

$$\mathcal{L}(f_m) = 10\log_{10}\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{f_0}{2Q_L f_m}\right)^2\right]\left[1+\frac{f_{1/f^3}}{f_m}\right]\right\} \tag{3-21}$$

where f_{1/f^3} is the $1/f^3$ corner frequency.

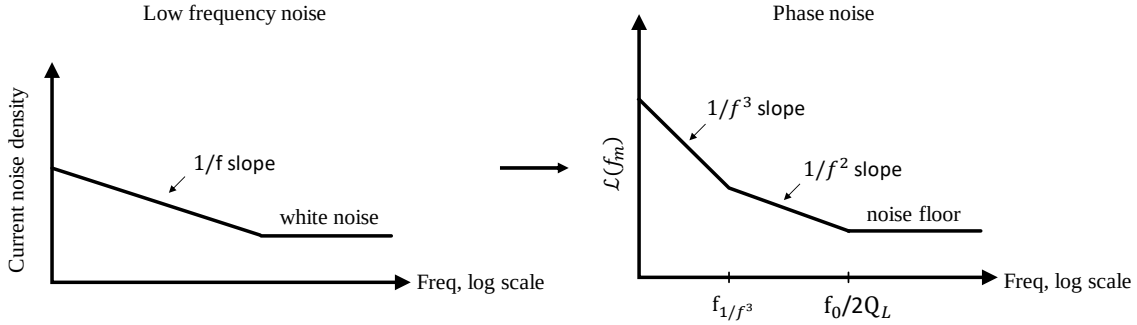


Fig. 3-5. Low frequency noise up-conversion into phase noise according to Leeson's equation.

Fig. 3-5 shows the low frequency noise up-conversion into phase noise according to equation (3-21). Based on Leeson's phase noise model in equation (3-21), the power swing over the tank and *Q*-factor should be maximized to have a low phase noise oscillator. Also in equation (3-21), the factor *F* is to adjust the level, it is determined from the measurement and cannot be predicted from circuit noise analysis [65].

Lesson's phase noise model is a Linear Time Invariant (LTI) model, assuming that noise is linear, only depending on bias currents and is up-converted without time-variance. However, real oscillators are time-variant systems. Hence, there is a need for a quantitative model which can predict time-variant circuit behaviours. A linear time variant (LTV)

model was demonstrated by A. Hajimiri and T. Lee in 1998 [65-67], enabling an accurate phase noise prediction. In this method, a periodic function, called impulse sensitivity function (ISF), is used to analyze the oscillator phase noise. The ISF, i.e. $\Gamma(\omega_0 t)$, is a periodic function with the period as same as the signal waveform. It can be expressed by Fourier expansion as

$$\Gamma(\omega_0 t) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n) \tag{3-22}$$

where c_n is real-valued coefficients and θ_n is the phase of nth harmonic.

In oscillator design, the ISF will be calculated from the circuit simulation. A method for ISF calculation based on Hajimiri's model is proposed in [68]. Once the ISF is known, the phase noise in 20 dB region and 30 dB region can be calculated. If the circuit has only thermal noise, the phase noise is given by

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right) \tag{3-23}$$

where $\Delta\omega$ is the small displacement from the angular oscillation frequency ω_0, q_{max} is maximum charge stored in the tank, Γ_{rms} is the rms value of the ISF, $\overline{i_n^2}/\Delta f$ is thermal noise modeled in equation (3-1).

For flicker noise up-conversion, the noise spectrum is calculated by

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{c_0^2}{q_{max}^2}\frac{\overline{i_{1/f}^2}/\Delta f}{2\Delta\omega^2}\right) \tag{3-24}$$

where c_0 is the dc value of the ISF, $\overline{i_{1/f}^2}/\Delta f$ is the *1/f* noise modelled in equation (3-4).

In Hajimiri's model, noise sources such as shot noise, flicker noise, are time-variant with the same periodicity as the oscillation. These cyclostationary noise sources are strongly depends on the signal waveform of the oscillator and can be expressed by stationary noise $i_{n0}(t)$ multiplied to the normalized periodic modulation function $\alpha(\omega_0 t)$

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t) \tag{3-25}$$

A new effective ISF is defined with the cyclostationary noise source as:

$$\Gamma_{eff}(\omega_0 t) = \Gamma(\omega_0 t) \cdot \alpha(\omega_0 t) \tag{3-26}$$

This effective ISF is used for accurate phase noise calculation in $1/f^3$ region based on equation (3-24).

3.3 Varactors

The frequency of the output signal from an oscillator design can be fixed or variable. For microwave applications, the design of a fixed frequency oscillator (FFO) is usually based on the resonant inductor (*L*) and capacitor (*C*) circuits which can be in series or in parallel.

In MMIC technology, the widely used inductor is spiral inductor and capacitor is metal-insulator-metal (MIM) capacitor. However, the size of spiral inductors might be large in many cases depending on the designed frequency or topology. In order to tune the oscillation frequency, the variable elements, e.g. variable inductor or variable capacitor (varactor) must be used. In MMIC, a varactor diode is commonly used to replace a MIM capacitor, enabling the tuning of the oscillation frequency. The varactor diode uses p-n junction (or metal-semiconductor junction) in the reverse bias and its capacitance is varied with a reverse applied voltage. The *C-V* relationship of a p-n junction diode is shown as

$$C_j(V_m) = C_0 \frac{1}{\left(1 - \frac{V_m}{\Psi_0}\right)^{\eta}} \tag{3-27}$$

where Ψ_0 is the built-in potential of the p-n junction, η is a factor depending on the doping profile in the p-n junction ($0.1<\eta<2$), V_m is the applied voltage.

Like a MIM capacitor, a varactor is not an ideal component since it always has parasitic components. The losses of passive elements is usually defined in term of quality factor and the quality factor of a varactor can be expressed as

$$Q(V) = \frac{1}{2\pi f_0 C_j(V) R_s(V)} \tag{3-28}$$

where f_0 is the resonance frequency, $C_j(V)$ and $R_s(V)$ are the bias dependent tunable capacitance and series resistance, respectively.

In general, the *Q*-factor of a varactor is lower than for a MIM capacitor. An oscillator design based on a varactor is called a voltage-controlled-oscillator (VCO). The tuning range of a VCO is associated with the ratio C_{max}/C_{min} of the varactor.

In practice, the *Q*-factor characterisation of a varactor is quite sensitive to measurement errors since it relies on the accuracy of the extracted parasitic resistance. An alternative method based on a resonant structure was proposed by Deloach in 1964 [69]. A Deloach structure is a through transmission line shunted with a series resonant circuit consisting of a microstrip line and a varactor connected in series to ground, as shown in Fig. 3-6.

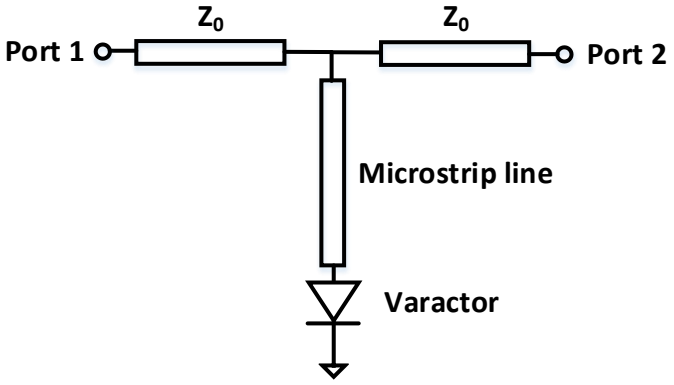


Fig. 3-6. Schematic diagram of a Deloach test structure.

The *Q*-factor at resonant frequency can be calculated from the 3 dB bandwidth of S_{21}, as seen in Fig. 3-7. The capacitance value of the varactor and other parasitic components can also be extracted from Deloach measurement as follow

$$R = (Z_0 / 2)\left(\frac{1}{\sqrt{T_p} - 1}\right) \tag{3-29}$$

$$C_j = \left(\frac{1}{\pi * Z_0}\right)\left(\frac{F_2 - F_1}{F_2 * F_1}\right)\left(\sqrt{T_p} - 1\right)\left(1 - \frac{2}{T_p}\right)^{1/2} \tag{3-30}$$

$$L = \left(\frac{1}{4 * \pi^2}\right)\left(\frac{1}{F_2 * F_1 * C_j}\right) \tag{3-31}$$

$$Q = F_{res} / (F_2 - F_1) \tag{3-32}$$

where Z_0 is the characteristic impedance of the transmission line, T_p is the power transmission loss ratio at resonance, F_1 and F_2 are two frequencies at 3 dB bandwidth, F_{res} is the resonant frequency.

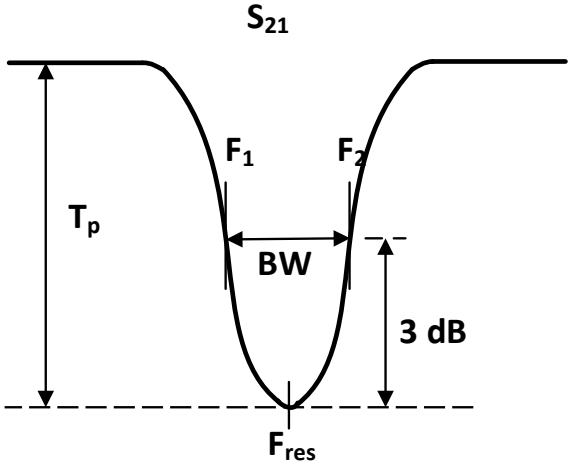


Fig. 3-7. Typical measured transmission loss (S_{21}) of a Deloach structure.

3.4 Oscillator specification and figures of merit

In the design of an oscillator, specific performance is targeted. Important parameters are summarised in Table 3-1.

Table 3-1. Summary of the performance parameters in oscillator design.

Property	Typical value
Oscillation frequency f_0	Depends on the applications
Tuning range	Depends on the applications
Output power P_{out}	around 0 – 5 dBm
Phase noise $\mathcal{L}(f_m)$	Depends on system's requirement. e.g. -110 dBc/Hz at 100 kHz offset is required for 4 MHz channel bandwidth of a system using 1024 QAM [70]
Harmonic suppression	> 20 dB
Tuning linearity	
DC power consumption P_{DC}	Varies with different transistor technologies.
Frequency pushing	In MHz/V
Frequency pulling	In MHz/load specification

In order to benchmark various oscillators, different figures of merit may be used [70]. It is difficult to define a single figure of merit for comparison of different transistor based oscillators which involve many performance parameters. A common figure of merit, *FOM* [71], which is a direct derivation of Leeson's equation normalized to power, consists of the oscillation frequency, the phase noise and the DC power consumption,

$$FOM = -\mathcal{L}_{meas}(f_m) + 20 * \log_{10}\left(\frac{f_0}{f_m}\right) - 10 * \log_{10}\left(\frac{P_{DC}}{1mW}\right) \quad (3\text{-}33)$$

where the $\mathcal{L}_{meas}(f_m)$is the measured phase noise at offset frequency f_m, f_0 is oscillation frequency, P_{DC} (mW) is DC power consumption.

In wireless communications, it is often more interesting to compare absolute performance rather than the performance normalized to power consumption. Thus, another figure of merit that enables a fair phase noise comparison of different oscillators operating at different frequencies and evaluated at different offset frequencies, that is [72],

$$\text{Normalized phase noise} = -\mathcal{L}_{meas}(f_m) + 20 * \log_{10}\left(\frac{f_0}{f_m}\right) \quad (3\text{-}34)$$

A higher normalized phase noise value indicates a better oscillator design concerning the $\mathcal{L}_{meas}(f_m)$ performance.

In practice, phase noise performance of VCOs are often worse than FFOs since the *Q*-factor of varactors are lower than MIM capacitors. Thus, another figure of merit allowing a fair phase noise comparison of tunable oscillators is introduced [72]

$$FOM_T = -\mathcal{L}_{meas}(f_m) + 20 * \log_{10}\left(\frac{BW}{f_m}\right) \quad (3\text{-}35)$$

where *BW* is the absolute tuning bandwidth. It should be noted that FOM_T is not applicable for FFOs that have very little tuning range.

Chapter 4

Characterisation & Modeling

This chapter presents details on characterisation and modeling. Section 4.1 presents the low frequency noise characterisation in which two types of LFN setups are described, followed by a benchmark of different transistor technologies. In addition, the investigations on the effects of different passivations and deposition methods and the variations of transistor geometry on the LFN for AlGaN/GaN based HEMTs and AlInN/GaN based HEMTs are also presented in section 4.1. Section 4.2 presents the characterisation of GaN HEMT varactors for the design of GaN HEMT VCO. Next, different techniques for phase noise measurements, i.e. cross-correlation methodology, phase detector methodology and direct spectrum measurement are presented in section 4.3. Section 4.4 presents flicker noise modeling and an accurate phase noise calculation using method in [68].

4.1 Low frequency noise characterisation

4.1.1 Low frequency noise setup

Two different setups are used for characterisation of LFN in this work, either based on a current-voltage amplifier or a voltage-voltage amplifier.

The first one, called setup A, was proposed the first time by Franz Sischka from Agilent Technologies [73]. In this setup, a current to voltage preamplifier from Stanford Research, SR570, is used, see Fig. 4-1. The collector current/drain voltage is biased from an internal voltage supply of the SR570 while the base current/gate voltage is biased through a parameter analyzer 4156 for accurate current/voltage control. A 1 Hz low-pass filter is used for the noise leakage elimination. The fast fourier transform (FFT) calculation is performed by the Dynamic Signal Analyzer (DSA). The LFN measurement range is from 1 Hz to 105.7 kHz which is limited by the bandwidth of the DSA. The measured noise current at the collector/drain side of device under test (DUT) is calculated by the multiplication of the measured noise voltage performed at the DSA and the sensitivity of the SR570. Thanks to the good noise floor of the internal bias from SR570,

i.e. 10^{-24} A^2/Hz, this setup is perfect for LFN measurement of low noise devices, e.g. HBTs, at low current/voltage bias.

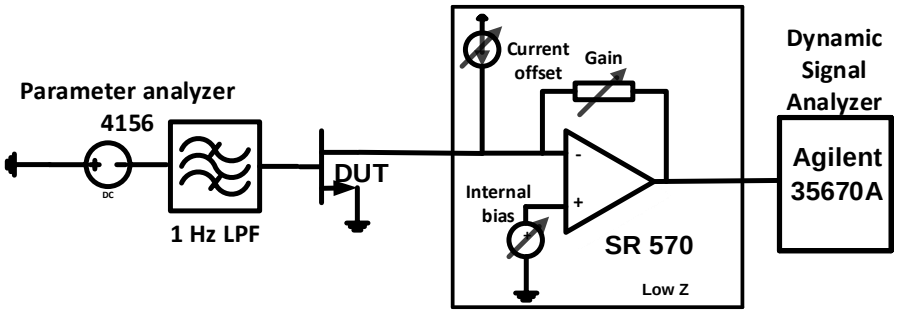


Fig. 4-1. LFN measurement setup based on current-voltage amplifier, SR570.

Setup A has a limitation is that the internal voltage supply of the SR570 cannot support a voltage larger than 4V and a current larger than 6 mA. Thus, an external bias tee is added in setup A, as seen in Fig. 4-2, to improve the voltage/current handling capability. Unfortunately, the additional bias tee has a cut-off frequency of 3 Hz, leading to a discontinuity in the LFN spectrum. Moreover, noise from the big electrolyte capacitors used in the bias tee increases the noise floor. The big capacitors also require long time for charging/discharging at every collector/drain bias point, leading to slow measurements and difficulties in automatic control of the setup. This setup is used in part of paper [A].

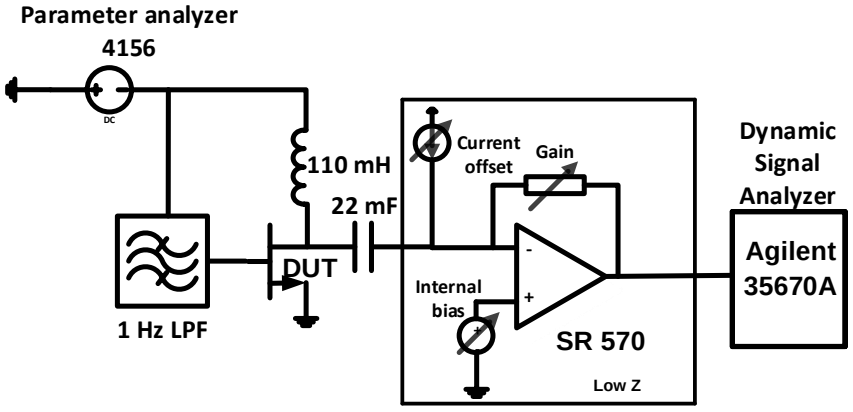


Fig. 4-2. Setup A with external bias tee.

An alternative solution to setup A completed with external bias tee that uses a voltage to voltage preamplifier from Stanford Research, SR560, is shown in Fig. 4-3. It is called setup B. In this setup, the gate voltage is biased from the SR570's internal supply and the drain voltage is biased from a parameter analyzer through a constant load resistor R_L of 110 Ω. First, the DC I-V measurement is performed. Then, the compensation for the voltage drop across R_L is calculated. In every measurement, the channel resistance R_{ds} also needs to be determined from the measured I-V curve ($R_{ds} = \Delta V/\Delta I$). Finally, the measured drain noise current is calculated by normalizing the measured drain noise voltage (which is performed in the DSA and multiplied to the sensitivity of the SR560) to the parallel

combination of resistances of R_{ds} and R_L. The two outputs from the SR570 and the SR560 are connected to a dual channel DSA, allowing the LFN measurement at the gate side as well. The accuracy of this method is very good in the forward-active region of the IV curve where R_L is dominating resistance over R_{ds}. It has been experimentally shown that minimum drain voltage of 2 V for GaN HEMTs and 0.5 V for GaAs pHEMTs can be measured with this setup. All measurements are controlled automatically with Matlab. Setup B is used to measure LFN of active devices in papers [A-D]. A Keysight's E4727A Advanced LFN analyzer (ALFNA) setup [74] is used for LFN characterisation of devices in paper [E]. The ALFNA system is operated in voltage amplifier mode with a functionally similar to setup B.

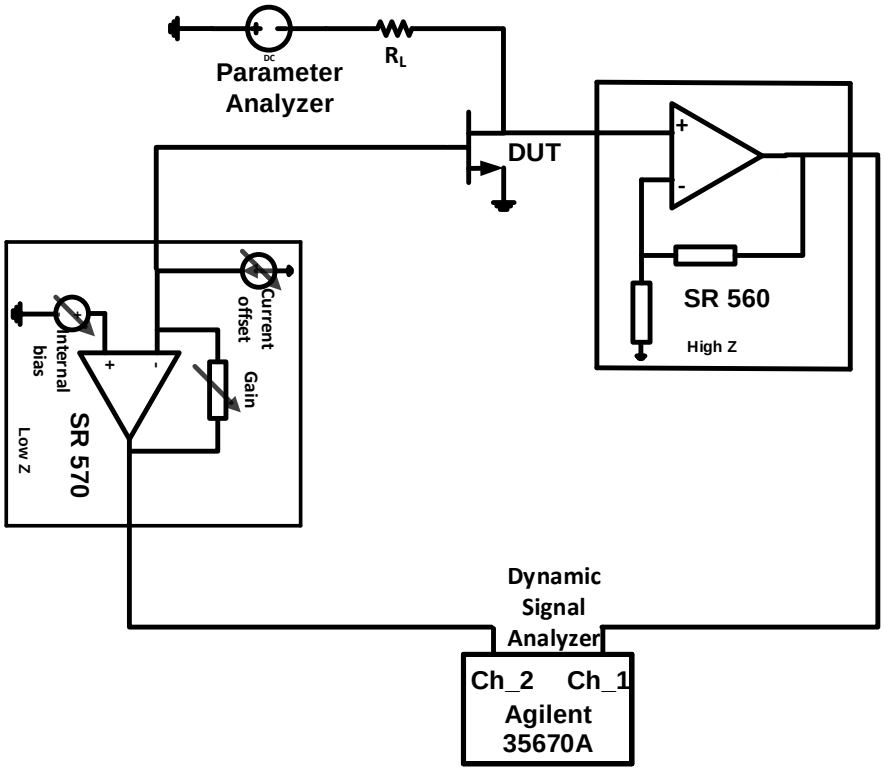


Fig. 4-3. LFN measurement setup based on voltage-voltage amplifier, SR560.

The setup verification is performed with a 4x125µm GaAs pHEMT from UMS technology with 220nm gate length. Its LFN level is characterised with the different measurement setups, i.e. setup A with external bias tee, setup B and setup B complemented with battery, for both low current and high current biases. At high current bias, the LFN results between the three setups agree very well, as performed in Fig. 4-4. It can be seen that its LFN does not have a clear *1/f* slope which is a sign of non-perfect crystal quality of the material. However, at low current bias, setup B is limited by the noise floor of the parameter analyzer as seen in Fig. 4-5. To enable LFN measurement below the noise floor level of the parameter analyzer 4156, a battery is used to replace the 4156, but then it limits the automatic bias control. Despite having limitation on the noise floor of the parameter analyzer, setup B is still preferred for measurements of devices having *1/f* noise levels higher than the noise floor of the 4156 such as GaN HEMT.

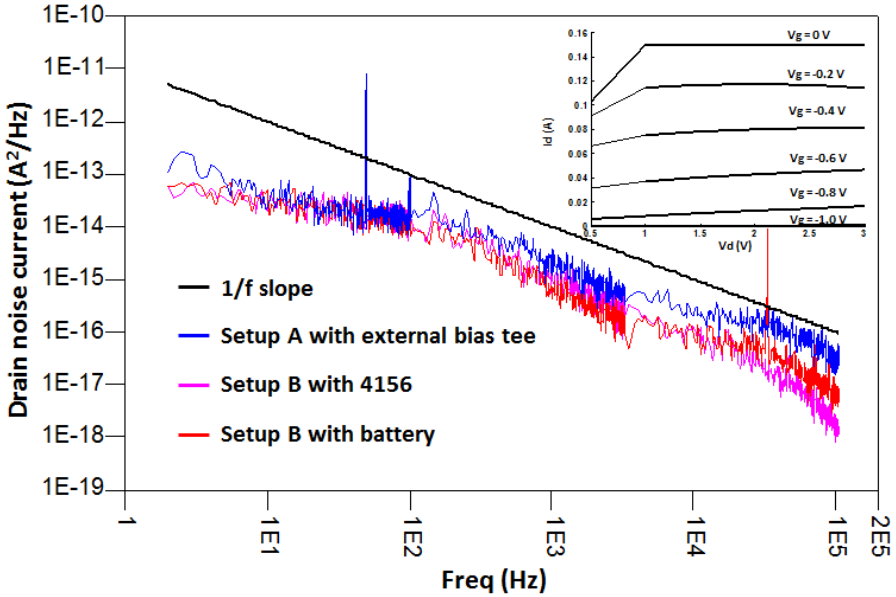


Fig. 4-4. LFN measurements of 4x125 μm pHEMT device versus the frequency with different measurement methods at V_d = 3V, V_g = -0.8V and I_d = 16 mA.

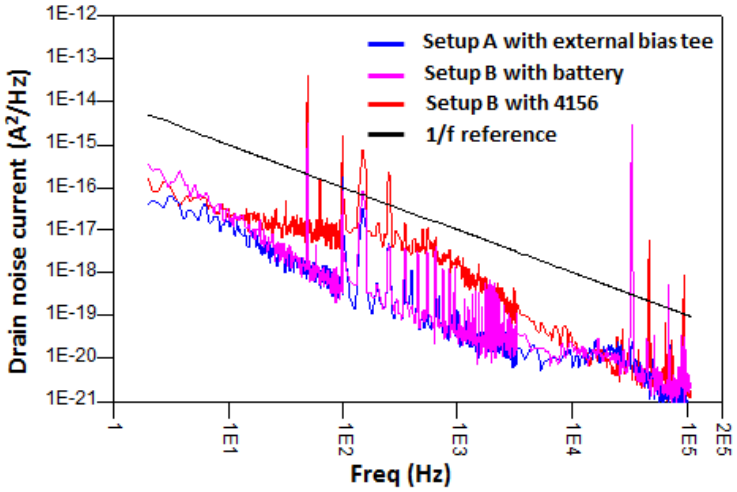


Fig. 4-5. LFN measurements of 4x125 μm pHEMT device versus the frequency with different measurement methods at V_d = 3 V, V_g = -1.2 V and I_d = 0.04 mA.

4.1.2 Benchmark of different transistor technologies

In this part, the LFN of some commonly used MMIC transistor technologies, e.g., GaAs-InGaP HBT, GaAs pHEMT and GaN HEMT are performed and compared, paper [A]. Setup A completed with external bias tee is used for LFN measurement of GaAs InGaP HBTs since they require a low noise floor while GaAs pHEMT and GaN HEMTs are

measured with setup B.

Fig. 4-6 shows a chosen LFN spectrum of a 4x20 µm GaAs-InGaP HBT with a collector voltage V_{cc} = 3V and a base current swept from 20 µA to 60 µA, corresponding to a collector current of 3 mA to 9 mA. It has been seen that the LFN increases with the collector current until the device is saturated. Moreover, LFN also increases with collector voltage.

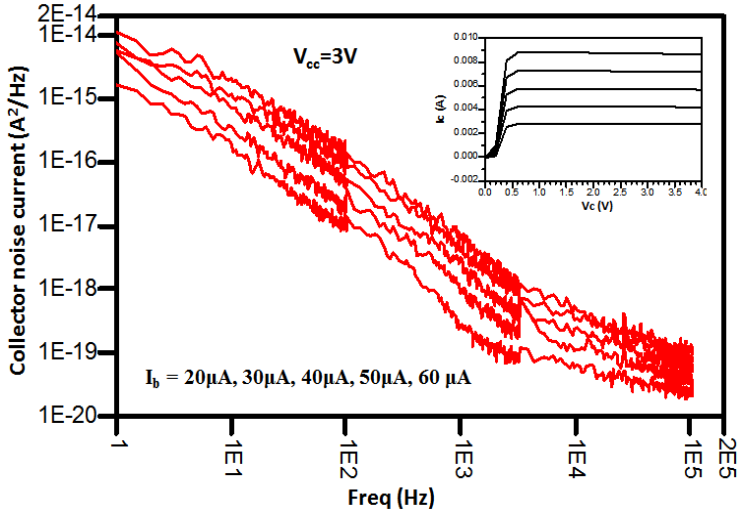


Fig. 4-6. Measured LFN spectra of a 4x20 µm GaAs InGaP HBT device from WIN Semiconductors technology for V_{cc} = 3V.

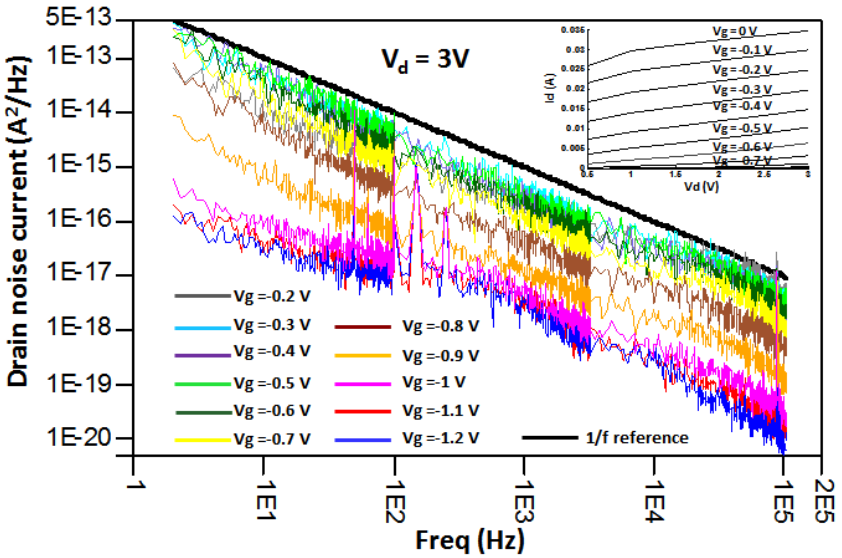


Fig.4-7. Measured LFN spectra of a 4x20 µm pHEMT with 150nm gate length, V_d = 3V.

Fig. 4-7 shows a LFN spectrum of a 150nm GaAs pHEMT device with 80µm gate-periphery versus the frequency at a drain voltage V_d = 3V and the gate voltage is swept from -1.2 V to -0.2 V. It is seen that the level of noise is higher compared to InGaP HBT, but the shape of the noise is very near the ideal *1/f* which indicates a good crystal quality of the material. Other GaAs pHEMT devices with 100 nm gate-length have also been measured. Their LFN level is higher than the 150 nm gate-length devices even though

their spectrum is similar, probably because the devices with shorter gate length have more defects along the gate.

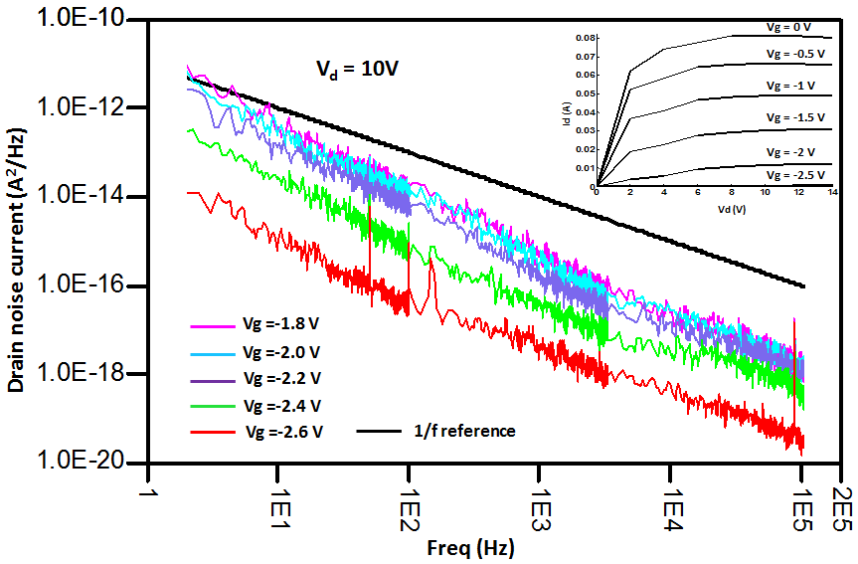


Fig. 4-8. Measured LFN spectra of a 2x75μm GaN HEMT with 250nm gate length, V_d = 10V.

Several GaN HEMT devices which have different dimensions (gate widths and number of fingers) from different vendors such as UMS, Qorvo, and Chalmers have also been measured. The drain voltages are held constant at 2 V, 6 V and 10 V while the gate bias is swept. Fig. 4-8 shows a typical LFN spectrum of a 2x75 μm GaN HEMT with 250 nm gate length at 10 V drain voltage. It is observed that the slope is steeper than *1/f*, which can be expressed as $1/f^{\gamma}$. Some previous works have shown that the slope of GaN HEMT, γ, varies from 1 to 1.3 [54]. But the slope in this experiment is even steeper, i.e. from 1.3 to 1.5.

The whole LFN data from all measured devices are summarised in Table 4-1. Note that the data listed in Table 4-1 are taken in the forward active region, where the flicker noise normalized versus power has its lowest value. The measured data in Table 4-1 verifies the well-known fact that bipolar devices have lower flicker noise compared to FET devices. However, these measurements are taken for quite different bias points, thus the measured noise level should be normalized versus power to have a fair comparison. With the target on oscillator applications, we may initiate from Leeson's equation, section 3.2.5. It is seen that oscillator phase noise is proportional to $(LFN)/P_s$. Assuming that oscillator is well designed and has a constant efficiency, a benchmark factor, i.e. $(LFN)/P_{DC}$, where P_{DC} is DC power consumption, is used in the comparison. It has been seen that GaN HEMTs have a better LFN-normalized-DC power value compared to GaAs pHEMTs. For instance, at 10 kHz the best GaN HEMT device demonstrates a benchmark parameter approximately five times better than the best GaAs pHEMT device, corresponding to an improvement of 7 dB in oscillator phase noise. The best performance in terms of absolute flicker noise levels is obtained for GaAs-InGaP HBTs. But at larger frequencies, e.g. 100 kHz, the best GaN HEMT device has lower LFN normalized power than the best InGaP HBT one. Therefore, GaN HEMT is considered as an attractive technology for oscillator design, in particular if phase noise at large offset frequencies where the shot noise may limit the bipolar devices is of concern.

TABLE 4-1
COMPARISON OF BENCHMARK PARAMETERS OF DIFFERENT DEVICES

Device	Size (µm)	L_g/W_e (nm)	y	Id (mA)	Vd (V)	LFN@1kHz (A^2/Hz)	LFN@1kHz $\frac{}{V_d \cdot I_d}$ (A/Hz.V)	LFN@10kHz (A^2/Hz)	LFN@10kHz $\frac{}{V_d \cdot I_d}$ (A/Hz.V)	LFN@100kHz (A^2/Hz)	LFN@100kHz $\frac{}{V_d \cdot I_d}$ (A/Hz.V)
GaN HEMT 1	2x75	250	1.5	19.252	10	4.26E-16	2.2143E-15	2.41E-17	1.253E-16	1.76E-18	9.1315E-18
GaN HEMT 2	4x75	250	1.3	27.376	10	2.27E-16	8.3065E-16	3.26E-17	1.19E-16	2.67E-18	9.7604E-18
GaN HEMT 3	2x50	250	1.3	20.037	10	6.75E-16	3.3678E-15	2.56E-17	1.275E-16	8.63E-19	4.305E-18
GaN HEMT 4	4x50	250	1.3	38.964	10	1.53E-15	3.9216E-15	6.66E-17	1.71E-16	1.75E-18	4.4965E-18
GaN HEMT 5	8x50	250	1.3	81.034	10	3.10E-15	3.828E-15	1.45E-16	1.784E-16	3.48E-18	4.2957E-18
GaN HEMT 6	4x50	250	1.5	4.732	10	4.50E-16	9.5139E-15	1.71E-17	3.618E-16	1.43E-19	3.0283E-18
GaN HEMT 7	8x50	250	1.5	52.604	10	2.79E-15	5.3114E-15	6.66E-17	1.265E-16	6.55E-19	1.2446E-18
InGaP HBT 1	4x20	1000	1.2	9	3	7.00E-18	3.8889E-16	5.30E-19	1.963E-17	1.10E-19	4.074E-18
InGaP HBT 2	2x20	1000	1.2	9	3	4.095E-18	1.5167E-16	4.538E-19	1.681E-17	1.324E-19	4.904E-18
GaAs pHEMT 1	2x20	150	1	12.611	3	1.42E-16	3.7507E-15	3.00E-17	7.924E-16	2.59E-18	6.8512E-17
GaAs pHEMT 2	4x20	150	1	24.833	3	1.87E-16	2.5101E-15	4.40E-17	5.911E-16	4.98E-18	6.682E-17
GaAs pHEMT 3	2x20	100	1	5.547	3	1.43E-16	8.6113E-15	2.00E-17	1.199E-15	2.64E-18	1.5852E-16
GaAs pHEMT 4	4x20	100	1	11.251	3	1.81E-16	5.3536E-15	3.35E-17	9.919E-16	3.85E-18	1.1412E-16
GaAs pHEMT 5	2x40	100	1	11.491	3	1.83E-16	5.3201E-15	2.76E-17	8.015E-16	4.06E-18	1.1786E-16
GaAs pHEMT 6	4x40	100	1	24.883	3	2.65E-16	3.5499E-15	3.88E-17	5.191E-16	4.71E-18	6.3055E-17

4.1.3 Low frequency noise studies

4.1.3.1 Surface passivation and deposition methods

This part investigates LFN behavior of AlInN/AlN/GaN HEMTs with different passivation methods, paper [B]. The LFN measurements are demonstrated for the devices on the three samples. One is passivated with Si_3N_4 and deposited with Plasma-Enhanced Chemical Vapor Deposition (PECVD). Two other pieces are passivated with the same Al_2O_3, but with two different deposition methods: plasma-assisted Atomic Layer Deposition (ALD) and thermal ALD. The devices are fabricated by Chalmers MMIC process, see section 2-1. All devices have the same size of 2x50 µm. Some data of devices are summarised in Table 4-2. The HEMTs used in this study have the same gate length (L_g) of 100 nm and source-drain distance (d_{SD}) of 1 µm.

TABLE 4-2
DEVICES IN THIS STUDY

	Thermal ALD HEMT	**Plasma ALD HEMT**	**PECVD HEMT**
Passivation	**Al_2O_3 by thermal ALD**	**Al_2O_3 by plasma-assisted ALD**	**Si_3N_4 by PECVD**
n_s [cm^{-2}]	1.529×10^{13}	1.602×10^{13}	1.663×10^{13}
R_{sh} [Ω/sq]	259	253	241
µ [$cm^2V^{-1}s^{-1}$]	1575	1540	1555
V_{po} [V]	-4.0	-5.0	-5.0

where n_s is carrier density, µ is mobility, R_{sh} is sheet resistance, V_{po} is pinch-off voltage.

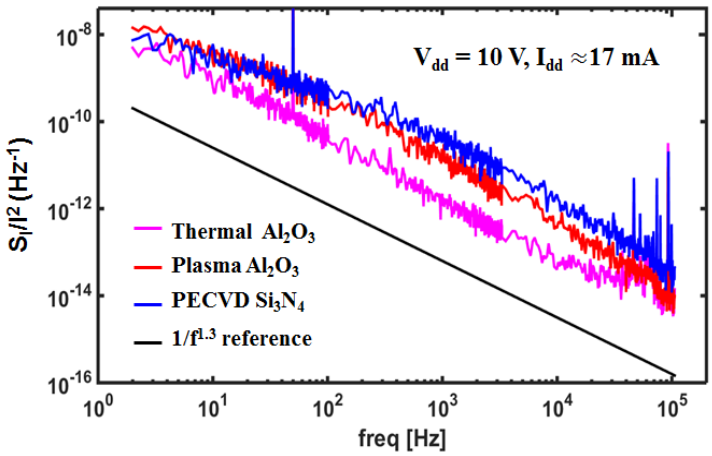


Fig. 4-9. Drain noise current spectra of the three AlInN/AlN/GaN HEMTs versus frequency at V_{dd} = 10 V, I_{dd} ≈ 17 mA.

With focus on oscillator applications, LFN characterisations in this study are performed under high drain voltage condition. The drain voltage is held at 10V while the gate bias is swept. The measured drain noise current spectral density S_I (A^2/Hz) normalized to the drain current squared (I^2) is used as LFN figure of merit. Fig. 4-9 shows the normalized drain current noise spectra (S_I/I^2) of the three AlInN/AlN/GaN HEMTs at a bias of V_{dd} = 10 V and $I_{dd} \approx$ 17 mA which is a reasonable operating point of an oscillator circuit. It can be seen the noise spectrum level of the sample passivated with Al_2O_3 by thermal ALD is significantly lower than for the two other samples. Furthermore, the noise spectrum of the thermally deposited Al_2O_3 HEMT has a nearly constant slope $1/f^{\gamma}$ with γ = 1.3 while the noise spectra of the plasma deposited Al_2O_3 and PECVD deposited Si_3N_4 HEMTs are more Lorentzian type, indicating the existence of deep level traps [57].

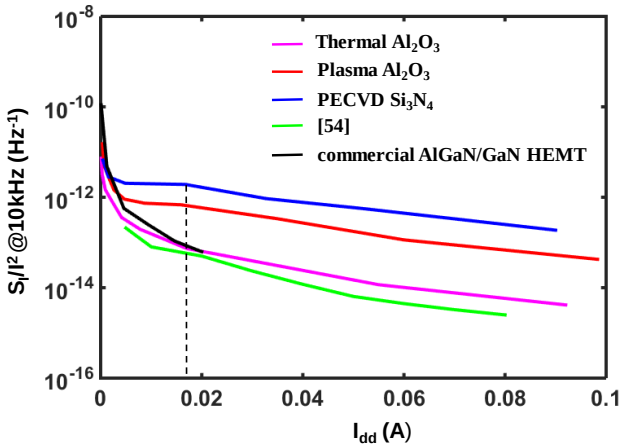


Fig. 4-10. Drain noise current spectra at 10 kHz versus the DC drain current of the three AlInN/AlN/GaN HEMTs at V_{dd} = 10 V, a 2×50 µm commercial AlGaN/GaN HEMT measured in paper [A] at V_{dd} = 10 V and an AlGaN/GaN device reported in [54] at V_{dd} = 5 V. The dashed line indicates $I_{dd} \approx$ 17 mA.

Fig. 4-10 shows the LFN spectral densities at off-set frequency 10 kHz versus DC drain current measured at V_{dd}=10 V of the three AlInN/AlN/GaN HEMTs, a commercial AlGaN/GaN HEMT measured in paper [A] and a state-of-the-art AlGaN/GaN HEMT published in [54]. There is no significant difference in noise performance between the three AlInN/AlN/GaN HEMTs for low drain currents. However, for larger drain currents, the thermal ALD Al_2O_3 HEMT presents 10 times lower noise compared to the plasma ALD Al_2O_3 HEMT and about 50 times lower noise compared to the PECVD Si_3N_4 HEMT. Assuming flicker noise as the dominant noise source, the 10-50 times improvement in noise spectral density would result in more than 10 dB improvement in oscillator phase noise [64]. The AlInN/GaN HEMT with thermal Al_2O_3 passivation also has a lower measured gate leakage current compared to the two other AlInN/GaN HEMTs, indicating a better LFN characteristic according to [43]. Furthermore, the noise level in AlInN/AlN/GaN thermal ALD HEMT is also in the same order of magnitude as AlGaN/GaN HEMTs. All results show that the thermal ALD AlInN/GaN HEMT is favored for oscillator applications.

4.1.3.2 Transistor gate length and source-drain distance

In this part, LFN measurements of AlInN/AlN/GaN HEMTs with variation in gate length (L_g) and source-drain (d_{SD}) distance are presented. The study is based on the sample passivated with Al_2O_3 plasma-assisted ALD mentioned in section 4.1.3.1. The measured devices have the same gate width (2x50 µm), but differ in L_g and d_{SD}. Three different gate lengths (L_g = 50, 100, 180 nm) and three different source drain distances (d_{SD} = 1, 1.5 and 2 µm) are investigated.

Fig. 4-11 present the measured drain noise spectra of the three AlInN/AlN/GaN HEMTs having the same d_{SD} of 1 µm, but different L_g, versus the frequency at V_{dd} = 10 V, $I_{dd} \approx$ 16 mA. The HEMT with longest gate length presents slightly higher LFN level at low frequencies, but in general there is not much difference in the noise level between the three devices.

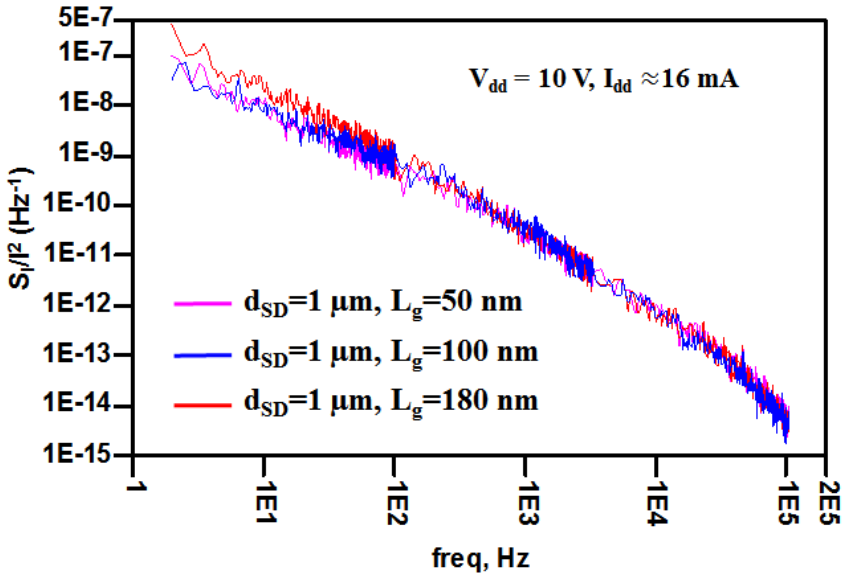


Fig. 4-11. Drain noise current spectra AlInN/AlN/GaN HEMTs with identical source drain distance but different gate length., at the bias condition is V_{dd} = 10 V, $I_{dd} \approx$ 16 mA.

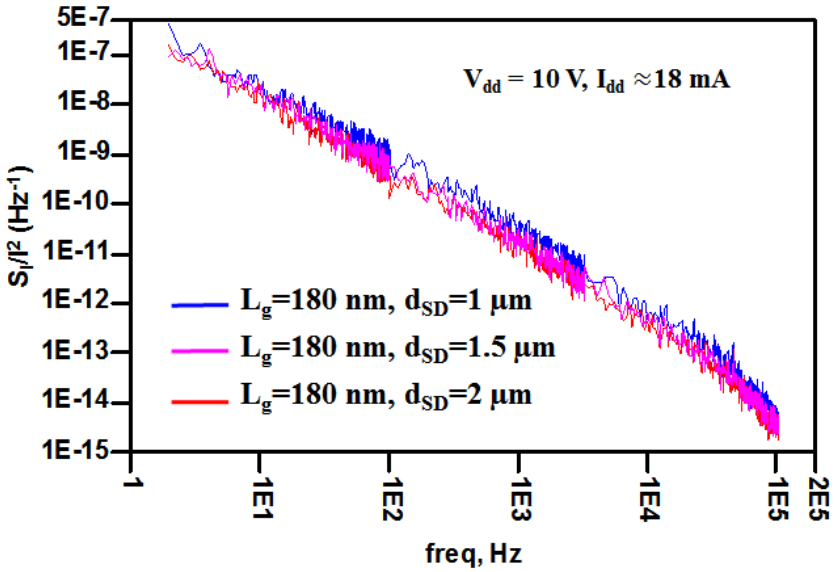


Fig. 4-12. Drain noise spectra of the three AlInN/AlN/GaN HEMTs having the same L_g of 180 nm, but having different d_{SD} of 1, 1.5 and 2 µm, respectively, versus the frequency at V_{dd} = 10 V, I_{dd} ≈ 18 mA.

Fig. 4-12 present the measured drain noise current spectra of the three AlInN/AlN/GaN HEMTs having the identical L_g of 180 nm, but different d_{SD} of 1, 1.5 and 2 µm, respectively, for a bias of V_{dd} = 10 V and I_{dd} ≈ 18 mA. The device with shortest d_{SD} has slightly higher LFN level compared to the two other HEMTs, but the difference is not significant.

In short, it is found that neither L_g nor d_{SD} affects considerably the LFN spectra of AlInN/GaN HEMT devices.

4.1.3.3 Transistor gate width

As already mentioned, LFN is up-converted to the phase noise around the microwave signal in an oscillator. With an oscillator designer, choosing the transistor size for the design is an important work, especially with GaN HEMT which has a relatively high LFN level. Therefore, there is a need to study LFN spectra transistors of different sizes. The devices used in this study are commercial AlGaN/GaN HEMTs from UMS Technologies. They have gate widths of 2x50, 4x50 and 8x50 µm, respectively.

Fig. 4-13 shows the drain current noise spectra (S_I/I^2) of the three AlGaN/GaN HEMTs with different width sizes at a bias of V_{dd} = 10 V and I_{dd} ≈ 20 mA. It can be seen that there is no significant difference in the noise spectra of these device. It seems that the LFN is scaled with the transistor size. Thus, the device geometry has only marginal effect on the LFN properties.

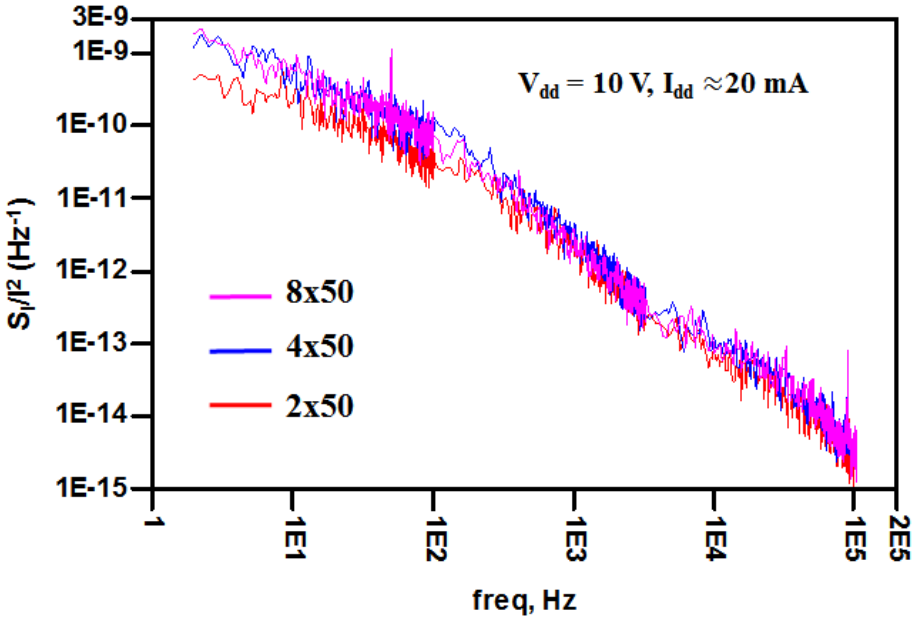


Fig. 4-13. Drain noise current spectra of the three AlGaN/GaN HEMTs with different gate width at V_{dd} = 10 V, I_{dd} ≈ 20 mA.

4.2 GaN HEMT Varactor characterisation

GaN HEMT varactors with various dimensions from UMS technologies are characterised with two-port *S*-parameter measurements, papers [C-D]. In HEMT process, the source and the drain of transistors are often intrinsic connected, forming the cathode while the gate acts as the anode of varactors based HEMT. An equivalent circuit of GaN HEMT varactor reported in [75] is used for the parameter extraction in which the effects of C_{gd} and R are negligible for simplicity, see Fig. 4-14. First, *S*-parameter measurements of the varactor at different bias voltages are carried out with a Vector Network Analyzer (VNA). The measured *S*-parameters is then converted to *Y*-parameters. The value of the intrinsic resistance R_j in the equivalent circuit is extracted by the real part of the admittance Y_{12} at resonance frequency. The value of capacitance C_j is calculated from the imaginary part of the admittance Y_{12} at low frequency where the inductance L can be negligible. Finally, the *Q*-factor is calculated based on equation (3-28). Fig. 4-15 (a) presents the simulated and extracted varactor capacitance $C_j(V)$ versus the tuning voltage at 10 GHz of the typical 8×50 GaN HEMT varactor based on two-port *S*-parameter measurements. It is seen that the extracted capacitance agrees quite well with the simulation. Fig. 4-15 (b) presents *Q*-factor $Q(V)$ versus the tuning voltage extracted at 10 GHz of the typical 8×50 GaN HEMT varactor based on two-port *S*-parameter measurements.

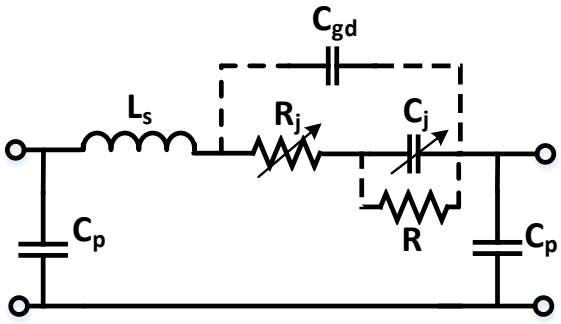
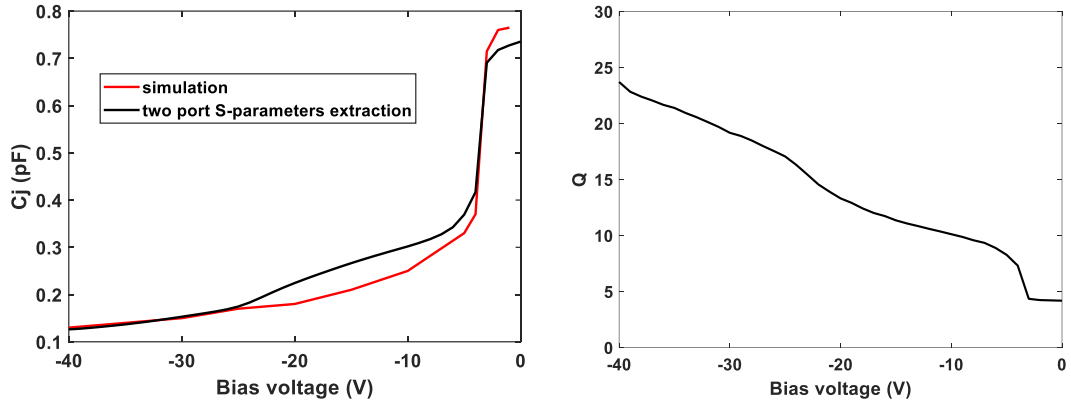


Fig. 4-14. An equivalent circuit of a GaN HEMT varactor in which the effects of C_{gd} and R are negligible for simplicity [75].



(a) (b)

Fig. 4-15. Characterisation of the 8×50 µm varactor based on two-port S parameter measurements. (a) simulated and extracted varactor capacitance at 10 GHz versus the bias voltage. (b) *Q*-factor extracted at 10 GHz versus the bias voltage.

Since the extracted *Q*-factor based on two port S-parameter measurements is often sensitive to measurement errors, a Deloach test structure for more accurate characterising of *Q*-factor of the 8×50 GaN HEMT varactor is also performed in this work. The details of the Deloach extraction are presented in section 3.3. Fig. 4-16 presents the varactor capacitance *C(V)* extracted from the two port structure and quality factor *Q(V)* extracted from a Deloach test structure versus the bias voltage at 10 GHz. It is seen that the *Q*-factor extracted from the Deloach test structure method has a higher value compared to the two port *S*-parameters method. As seen in Fig. 4-16, the useful tuning range is defined to be between -5 V to -40 V. The ratio C_{max}/C_{min} of this varactor is around 2.5 which is good for realising a medium tuning range VCO. Below -25 V, the capacitance variation of the varactor decreases significantly.

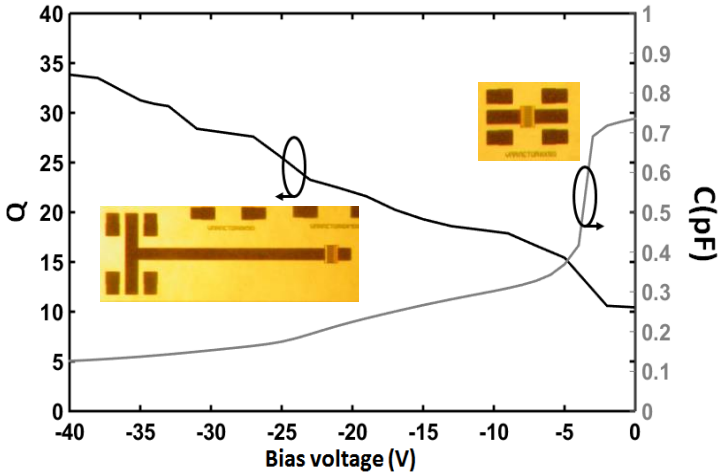


Fig. 4-16. Varactor capacitance extracted with two port structure and Q-factor extracted with Deloach test structure at 10 GHz versus the bias voltage of the 8×50 µm varactor.

4.3 Phase noise characterisation

There are different types of techniques to characterise the phase noise of an oscillator, e.g. direct spectrum measurement, phase detector methodology and cross-correlation methodology.

4.3.1 Direct spectrum measurement

The direct spectrum method is the most basic, oldest and simplest phase noise measurement [76]. The phase noise is simply characterised with an ordinary spectrum analyzer. As an example, the designed oscillators in this work are characterised using an FSUP50 signal-source analyzer up to 50 GHz from Rohde & Schwarz. The DUT is directly connect to the input of the signal source analyzer and the analyzer is tuned to the carrier frequency. Since single-sideband (SSB) phase noise $\mathcal{L}$ is defined as the normalized noise power within a 1 Hz bandwidth at an offset frequency f_m, the measured phase noise is calculated as follow

$$\mathcal{L}(f_m) = Pn\ (RBW)\ - Ps - 10\times log10(RBW) \qquad (4\text{-}1)$$

where P_s is carrier signal power and P_n is the noise power within the resolution bandwidth (*RBW)* at offset f_m.

It should be noticed that the noise floor of the spectrum analyzer should be lower than the measured phase noise of a DUT at offset frequencies of interest and the resolution bandwidth cannot be chosen lower than the lowest offset frequency for characterisation. For characterising a free-running oscillator >100 GHz, this method is preferred due to the lack of sufficiently good phase detectors and reference signals above 100 GHz. In this work, phase noise characterisation in papers [E] and [G] use this method.

4.3.2 Phase detector methodology

The main concept of this method is using a phase detector to isolate phase noise from amplitude noise. In general, the phase detector will compare and convert the phase difference between two inputs into a voltage. When two inputs have the 90 degree phase difference, the output of phase detector is 0 V and this point is called quadrature point [76]. Any phase variations around this quadrature point will result in a voltage fluctuation at the output of the phase detector. Then, the output voltage fluctuation of the phase detector can be digitally processed to get the phase noise information wanted. This method is often based on measuring two signal sources (DUT and a reference source) or only a single source (DUT). The first technique called Phase lock Loop (PLL) method uses a balanced mixer as phase detector and a PLL so that the reference source can follow the DUT at the same frequency and maintain the 90 degree phase difference between the two sources, see Fig. 4-17 [76]. The low pass filter (LPF) helps to filter out the mixing sum frequency 2 f_c and the output frequency is mixing difference frequency which is 0 Hz with an average voltage of 0 V. The output voltage fluctuation is then processed by a baseband analyzer to obtain the phase noise information. This method usually requires a clean tunable reference source and the phase noise of the reference signal limits the phase noise measurement range of DUT. In modern commercial spectrum analyzers, e.g. R&S FSUP 50, there are automatic routines for stepping the frequency and adjusting the resolution bandwidth to synthesize the phase noise spectrum versus off-set frequency. Papers [C], [D] in this work use this method.

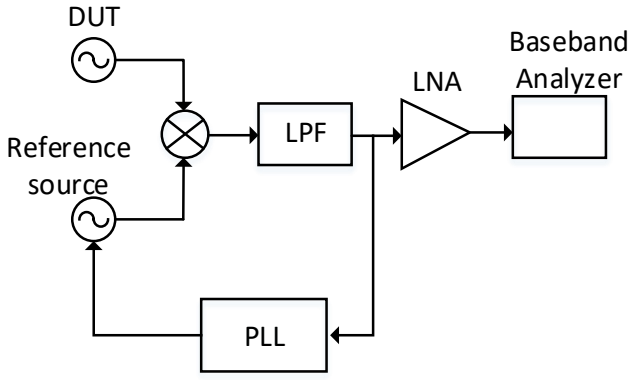


Fig. 4-17. Phase noise characterisation based on the PLL method.

The latter technique called frequency discriminator method needs only one source, i.e. DUT, as seen in Fig. 4-18 [76]. In fact, the reference source in PLL method is removed and the signal from the DUT is compared with a time delayed version of itself. The DUT signal is first split into two paths and the signal from one path is delayed compared to the other by a delay line converting frequency fluctuations to phase fluctuations. The signal from the other part goes through a phase shifter to adjust the inputs of the two parts to 90 degree phase difference for maximum sensitivity in the phase detector. As in the PLL method, the phase detector is normally implemented as a balanced mixer that converts the phase fluctuations to voltage fluctuations. The output voltage fluctuations are then analysed by the baseband analyzer to get the phase noise. Besides the advantage of no

need for a reference oscillator, the discriminator method has some drawbacks compared to the PLL method. First, the analog delay line limits the measurement sensitivity, particularly close-in offset frequency. A longer delay line can improve sensitivity, but can also limit a maximum offset frequency measured. Second, this method often requires a manual tuning of the phase shifter or the delay line in order to measure the phase noise at particular offset frequency. Thus, it does not have automatic routine which is inefficient for phase noise characterisation of oscillators at many points.

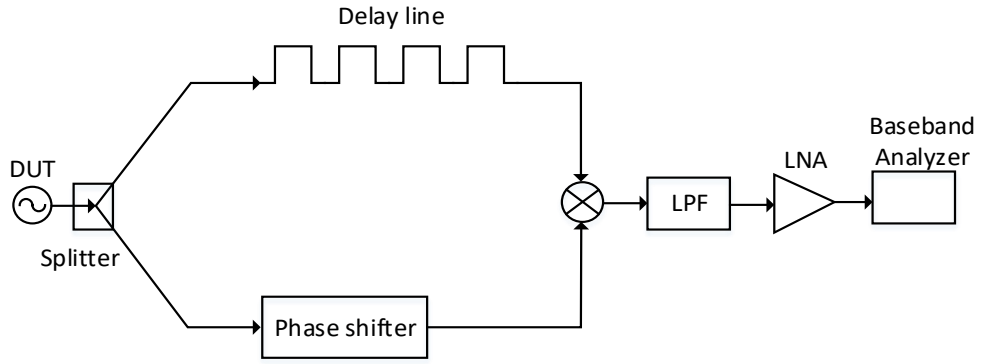


Fig. 4-18. Phase noise characterisation based on the frequency discriminator method.

4.3.3 Cross-correlation methodology

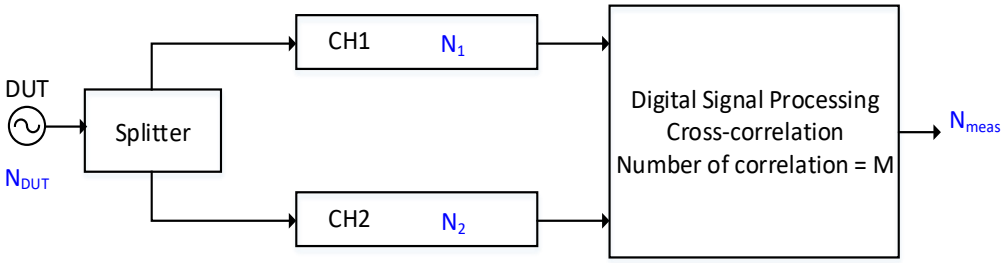


Fig. 4-19. Phase noise characterisation based on the cross-correlation method.

As discussed above, the PLL method is often limited by the performance of the reference source. Thus, in order to reach a low noise floor, i.e. 10 to 15 dB below the noise floor of the reference signal, the cross-correlation technique is utilised by two channel PLL systems as shown in Fig. 4-19 [76]. For example, the R&S FSUP 50 signal source analyzer used in this work has that dedicated hardware. The signal from DUT is split into two parts. Each of part goes through a PLL channel as already described in PLL method part. Assuming that system noise N_1 and N_2 are uncorrelated, the measured noise N_{meas} is calculated as follow

$$N_{meas} = N_{DUT} + (N_1 + N_2)/\sqrt{M} \qquad (4\text{-}2)$$

With correlation point $M=100$, the noise on (N_1+N_2) is improved 10 dB. However, the measurement speed is degraded when the number of correlation M increases.

4.4. Flicker noise modeling and accurate phase noise calculation

The MMIC oscillators in this work are designed with Harmonic Balance (HB) tool in Agilent's Advanced Design System (ADS). However, the phase noise simulation in HB only works fine when there is no flicker noise in the active device. To accurately predict the phase noise, this work addresses the method proposed in [68] of oscillators designed, papers [C-E]. To apply this method, a LFN measurement and oscillator waveforms from HB, i.e. transistor intrinsic current, tank resonance current, tank resonance voltage, are required. It should be noticed that this method only applies for LC feedback oscillator and the accuracy of this method will be less if the intrinsic current is inaccessible. Step by step to perform the calculated phase noise based on time-invariant method is described in [77].

Based on the measured LFN data, the flicker noise is modeled as in equation (3-4). Fig. 4-20 shows an example of the measured LFN of the 2×50 µm HEMT in paper [C] and its *1/f* noise model at V_d = 6 V and V_g is swept from -3.8 to -2.8 V. The extracted values of fitting parameters in the flicker noise model are:

$K_f = 1.3\times10^{-10}$, $A_f = 0.8$, $F_{fe} = 1.3$.

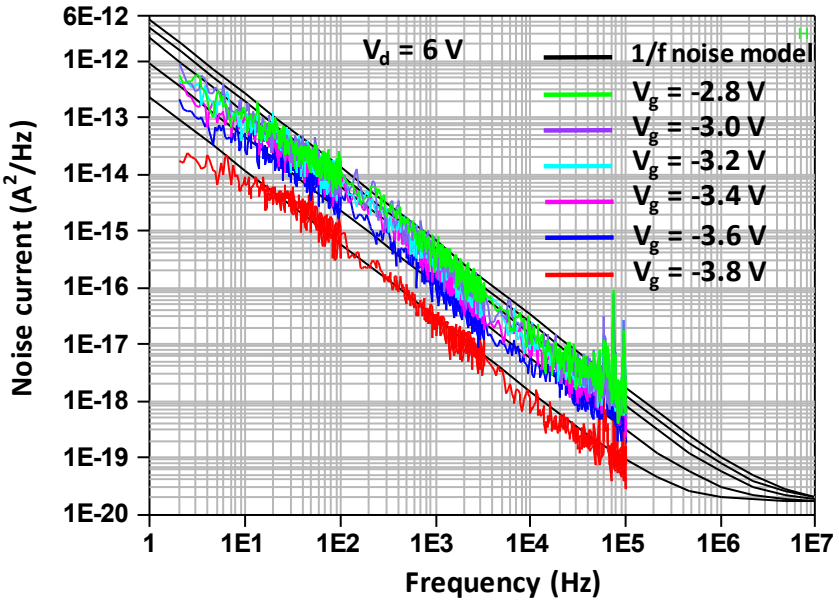
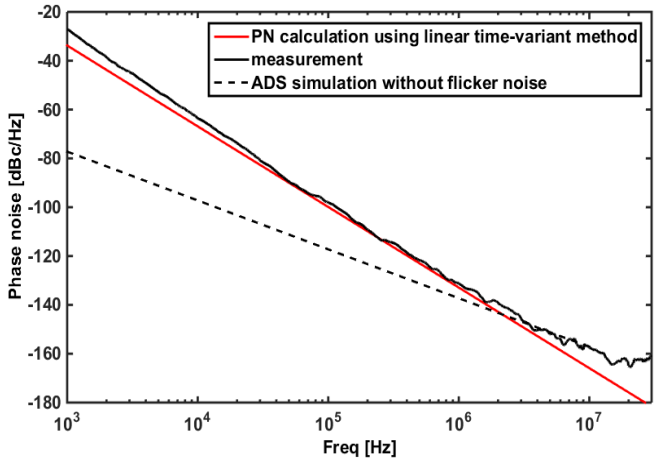
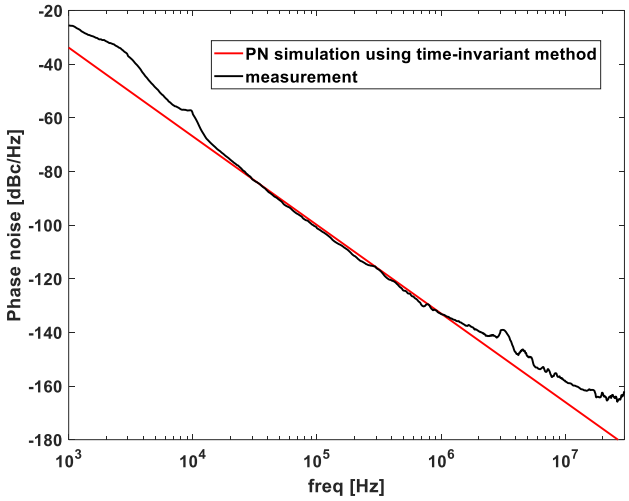


Fig. 4-20. Measured low frequency noise of the 2×50 µm HEMT and *1/f* noise model at V_d = 6 V, V_g is swept from -3.8 to -2.8 V.

Fig. 4-21 (a) and (b) show the simulated phase noise using time-invariant method [68] and the measured result at varactor voltage of V_v = 28.5 and 44 V for both VCO designs in paper [C] and paper [D], respectively. It can be seen that they agree very well in $1/f^3$ region.



(a)



(b)

Fig. 4-21. Measured phase noise versus offset frequency compared to simulated phase noise using time-invariant method [68]. (a) at a varactor voltage of V_v = 28.5 V for the VCO in paper [C]. (b) at V_v = 44 V for the first VCO in paper [D].

Chapter 5

MMIC design, simulations and measurement results

In this chapter, the MMIC design, simulations and measurements results of low phase noise signal sources in different transistor technologies such as GaN HEMT, InP DHBT, SiGe BiCMOS are presented. In section 5.1, the design of low phase noise GaN HEMT based oscillators including X-band VCO chip set (7-13 GHz) and Ka-band (23 GHz) reflection type oscillator with state-of-the-art phase noise performance are demonstrated. Section 5.2 presents a low phase noise 220 GHz oscillator in 130 nm InP DHBT technology with state-of-the-art performance. Finally, a low phase noise D-band signal source based on the Ka-band GaN HEMT oscillator presented in section 5.1 and SiGe MMIC integration of a sixtupler and an amplifier are shown in section 5.3. The signal source has lowest phase noise at 10 MHz offset reported for a D-band signal source.

5.1 Low phase noise oscillator design in GaN HEMT technology

5.1.1 X-band VCO chip set

This section presents the designs of X-band MMIC GaN HEMT based VCOs, papers [C], [D]. They are implemented in UMS's GH25-10 GaN HEMT process presented in section 2.1. The chosen topology for all of them is common gate balanced Colpitts, see Fig. 5-1, which is known for providing low phase noise and wide tuning range [78]. In Figs. 5-2 (a) and 5-2 (b), respectively, the chip photos of the designed VCOs in paper [C] and [D] are shown. The VCO presented in paper [C] shows the feasibility of a medium tuning range (> 15%) and low phase noise MMIC VCO in GaN HEMT technology while the GaN HEMT based VCO chip set designed in paper [D] covers a wide continuous frequency range from 7 to 13 GHz and aims for the use in X-band satellite converters. In paper [C], the transistor size used in the designed VCO is 2×50 µm while the transistor

size used for the VCO chip set in paper [D] is 2×100 µm. The component values in the schematic of each VCO are chosen for optimum phase noise and a big varactor size of 8×50 µm is also chosen for wide tuning range in all designs. Due to the limitation of varactor dimensions, two varactors are combined in parallel for VCOs at lower frequency bands in order to reach the desired capacitance value. In all circuits, the RF output signal is extracted through a MIM capacitance of 0.1 pF at one side, not only providing sufficient output power but also preventing the oscillator from being loaded by the measurement system, while the other RF port is left open. The bias point for each VCO is carefully optimised to minimise up-conversion of low frequency noise. All VCOs are designed with Agilent Advanced Design System (ADS) and are characterised using an FSUP 50 signal-source analyzer from Rohde & Schwarz. The low noise internal bias supplies of the FSUP are used for gate and drain biases while the varactor voltage is controlled from a Keithley power supply. Besides, time-variant phase noise predictions presented in section 4.4 are combined in each design.

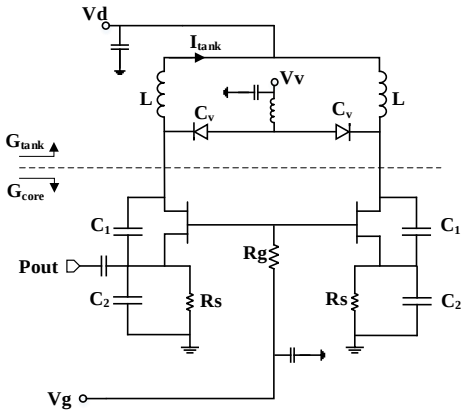
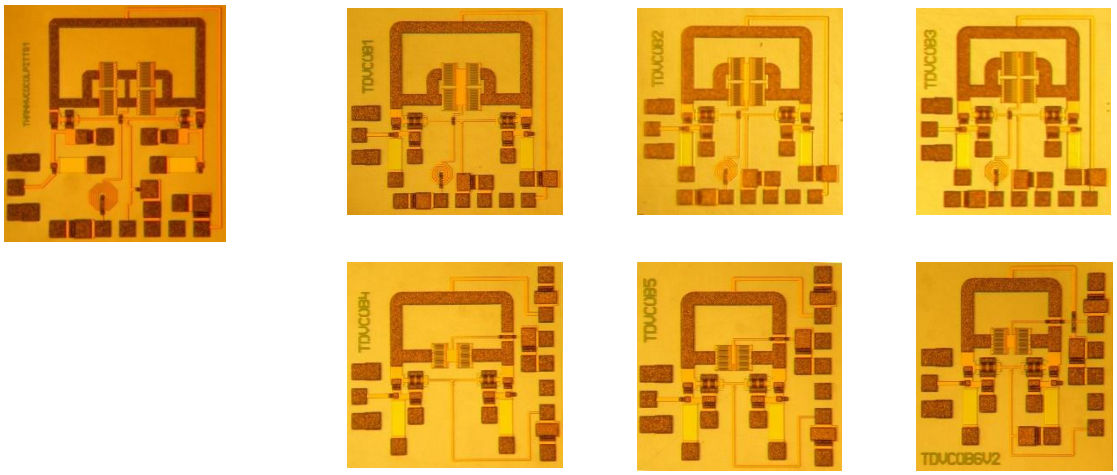


Fig. 5-1. Schematic of balanced Colpitts GaN HEMT VCO

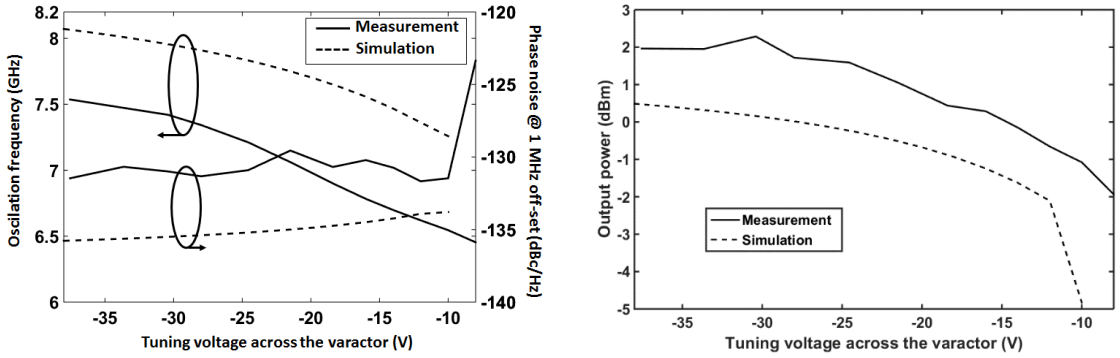


(a) (b)

Fig. 5-2. Chip photo of the designed Colpitts GaN HEMT VCOs. (a) Paper [C]. (b) Paper [D].

Fig. 5-3 (a) and (b) present the measured oscillation frequency and phase noise at 1 MHz offset and output power of the designed VCO in paper [C], respectively, versus varactor voltage compared to ADS simulation. The gate and drain voltages are held

constant at optimum points, i.e. -2 V and 6 V, respectively, while tuning voltage across the varactor is swept from -8 V to -38 V. The varactor characterisation is shown in section 4.2. It can be seen that the tuning shape agrees well between measurement and simulation. The measured oscillation frequency of the VCO is shifted down roughly 10% compared to simulation, probably due to parasitic capacitance. The measured output power of the VCO varies from -2 to 2 dBm which is 1.5 dB higher than the simulated. A tuning bandwidth of 1.1 GHz (6.45-7.55 GHz) is obtained, corresponding to a tuning range about 15%. The lowest 1 MHz offset phase noise performance is -132 dBc/Hz at a tuning voltage of V_v = -28.5 V.



(a) (b)

Fig. 5-3. Measurement and simulation result of the VCO in paper [C]. (a) Oscillation frequency and phase noise versus varactor tuning voltage. (b) Output power versus varactor tuning voltage.

Similarly to the measured VCO in paper [C], the bias point for the VCO chip set designed in paper [D] are fixed at the optimum point. Fig. 5-4 shows the measured and simulated oscillation frequency and phase noise at 100 kHz and at 1 MHz versus varactor bias voltage for the first VCO (the lowest frequency band) in paper [D] at V_{gg} = -2.5 V, V_{dd} = 6 V, Vv = 10 to 50 V. The measured oscillation frequency is shifted down roughly 5% compared to simulation, probably due to parasitic capacitance. The measured phase noise agrees well with the simulation that based on the cyclo-stationary model reported in [68] and presented in section 4.4. Note that the phase noise calculation applies for large offsets. The lowest phase noise achieved is -103 and -135 dBc/Hz at 100 kHz and 1MHz offset frequencies, respectively, for a varactor tuning voltage of V_v = 34 V.

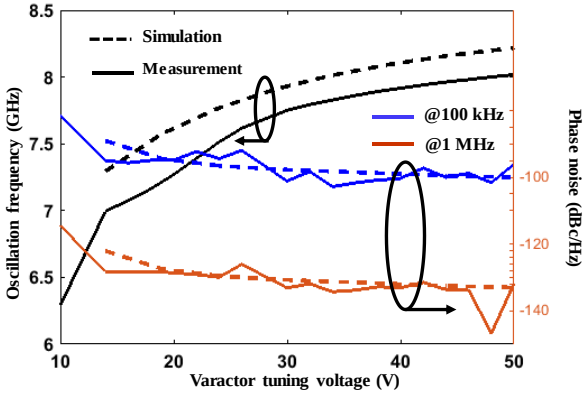
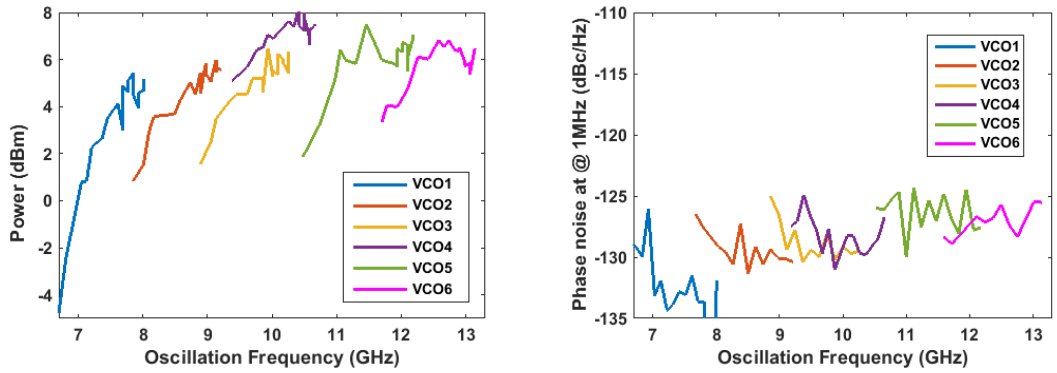


Fig. 5-4. Measured and simulated oscillation frequency and phase noise versus varactor tuning voltage for the first VCO in paper [D].

Fig. 5-5 (a) and (b) presents the measured RF power and the measured phase noise at 1 MHz off-set, respectively, of all VCOs in paper [D] versus oscillation frequency. It can be seen that the power over the large continuous frequency range from 7 to 13 GHz is maintained near the design target of 5 dBm which is sufficient for satellite transponders and the 1 MHz offset phase noise is maintained lower than -125 dBc/Hz. Each VCO has tuning range with the bandwidth better than 1 GHz.



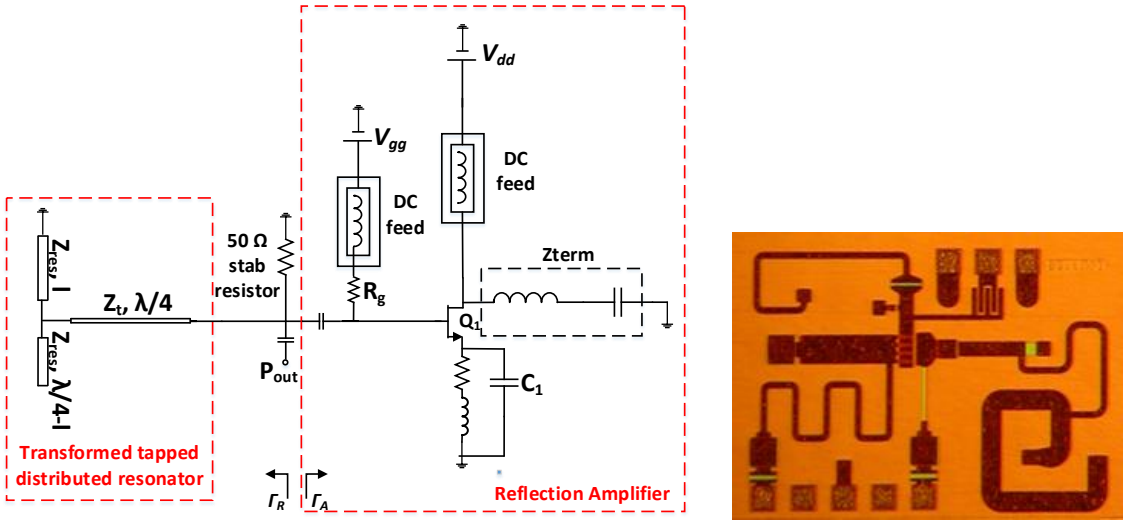
(a) (b)

Fig. 5-5. The VCOs in paper [D]. (a) the measured RF power versus oscillation frequency. (b) the measured phase noise at 1 MHz off-set of all versus oscillation frequency.

5.1.2 23 GHz reflection type oscillator

This section shows the design of a 23 GHz GaN HEMT reflection type oscillator (negative resistance oscillator), paper [G]. The oscillator is designed and fabricated in Qorvo's 0.15 µm AlGaN/GaN HEMT technology, see section 2.1. Fig. 5-6 (a) and (b) shows the schematic and chip photo, respectively, of the designed 23 GHz GaN HEMT-based oscillator. The oscillator consists of a reflection amplifier which is based on integrated HEMT device with inductive termination at drain and an integrated resonator is based on distributed transmission lines. In this reflection type oscillator, a fully distributed transformed tapped resonator, i.e. a lumped parallel resonator transformed through a high-impedance $\lambda/4$ line, proposed in [79] is implemented. In fact, the lumped MIM capacitor of the transformed resonator in [79] is replaced with an open stub, see Fig. 5-6. The tapping position and the width of the impedance transformer are adjusted to meet the impedance conditions. The circuit is designed in ADS. The simulated 1-port S-parameters of the reflection amplifier is optimised with a reflection gain of 8 dB at 23 GHz, corresponding to a reflection coefficient of Γ_A = -2.5 or a negative resistance of R_A = -21 Ω. Then, the resonator is tuned for optimum phase noise and sufficient gain margin. The final design has a total loop gain of 3 dB, corresponding to a reflection loss of 5 dB for the passive resonator that is obtained for a quarter-wave transformer impedance of Z_t = 71 Ω and a tune-length of $l = \lambda/8$. The designed resonator is also EM-simulated and obtained an unloaded quality factor of Q = 27, which is good value for an integrated MMIC oscillator at 23 GHz. As seen in Fig. 5-6, a 50 Ω resistance is added in parallel with the resonator to

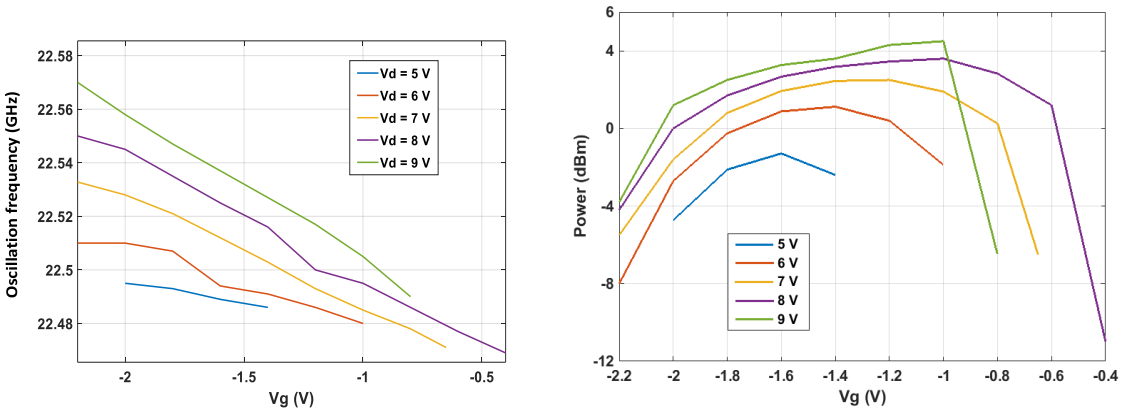
suppress unwanted resonances outside the desired frequency of oscillation. The output power is coupled from a small capacitor of 0.05 pF at the source.



(a) Schematic (b) Chip photo

Fig. 5-6. Schematic and chip photo of negative resistance GaN HEMT oscillator.

The designed 23 GHz GaN HEMT oscillator is characterised on-chip using the R&S FSUP. The gate and drain bias voltages are controlled from a Keithley power supply. Fig. 5-7 (a) shows the oscillation frequency versus the gate biasing with drain bias voltage as a parameter. The oscillation frequency is shifted down about 4% compared to the simulated result, i.e. 23.5 GHz, and the output power is varied from -11 to 4.5 dBm for all swept bias points, see Fig. 5-7 (b). Fig. 5-8 presents the measured phase noise versus offset frequency. The lowest measured phase noise at 100 kHz and 1 MHz off-set is -99 dBc/Hz and -129 dBc/Hz, respectively, at V_{dd} = 5 V and V_{gg} = -1.4 V, i.e., exactly -30 dB/decade slope indicating that the performance is limited by flicker noise. Outside 3 MHz the slope nearly approaches -20 dB/decade as seen in Fig. 5-8.



(a) (b)

Fig. 5-7. Oscillating frequency and output power of the 23 GHz GaN HEMT reflection type oscillator at different drain bias voltages versus the gate bias voltage.

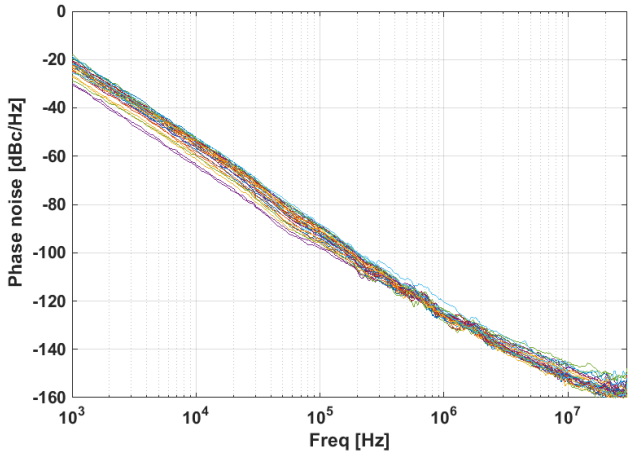


Fig. 5-8. Measured phase noise of the 23 GHz GaN HEMT reflection type oscillator versus offset frequencies.

5.1.3. Comparison to state-of-the-art III-V MMIC oscillators

Table 5-1 shows the comparison of GaN oscillators in paper [C], [D] and [G] to other state-of-the-art MMIC III-V oscillators reported in open literature.

TABLE 5-1
COMPARISON TO OTHER STATE-OF-THE-ART MMIC III-V OSCILLATORS

Ref.	Process	f_o (GHz)	P_{out} (dBm)	Min PN@100 kHz	Min PN@1 MHz	Normalized PN*@ 1 MHz	FOM_T**@ 1MHz
[68]	GaN HEMT	9.1	6	-101	-130	209	N/A
[80]	GaN HEMT	9.9	17	-105	-135***	215	N/A
[36]	GaN HEMT	9.92	-6	-109	-136	216	N/A
[37]	GaN HEMT	15.05	-6	-106	-133	216	N/A
[35]	GaN HEMT	6.5-7.5	2	-81	-110	187	170
[81]	InGaP HBT	25	-1	-106	-130	218	N/A
[78]	InGaP HBT	6.35-6.5	5.5	-112	-138	214	N/A
[72]	InGaP HBT	8.0-9.7	7	-106	-128	208	193
[82]	InGaP HBT	6.1-7.5	-5	-102	-125	202	188
This work, paper [C]	**GaN HEMT**	**6.45-7.55**	**2**	**-98**	**-132**	**209**	**193**
This work, paper [D]	**GaN HEMT**	**7-8**	**2**	**-100**	**-135**	**212**	**195**
This work, paper [D]	**GaN HEMT**	**7.8-9.1**	**3.7**	**-98**	**-130**	**209**	**192**
This work, paper [D]	**GaN HEMT**	**8.9-10.2**	**4**	**-96**	**-129**	**209**	**191**
This work, paper [D]	**GaN HEMT**	**9.3-10.6**	**6.5**	**-97**	**-129**	**209**	**191**
This work, paper [D]	**GaN HEMT**	**10.5-12.1**	**4**	**-95**	**-127**	**208**	**191**
This work, paper [D]	**GaN HEMT**	**11.5-13.1**	**5**	**-95**	**-127**	**209**	**191**
This work, paper [G]	**GaN HEMT**	**22.5**	**1**	**-99**	**-129**	**216**	**N/A**

* & ** Normalized phase noise and FOM for tunable oscillators presented in section 3.4.
*** Extrapolated by 30 dB/decade.

At near carrier offsets such as 100 kHz, the phase noise performances of GaN HEMT-based oscillators are higher than InGaP HBT-based oscillators. However, at 1 MHz offset, phase noise performances of the designed X-band GaN HEMT VCOs are slightly better than state-of-the-art MMIC X-band GaAs-InGaP HBT VCOs for comparable frequency and tuning range. They are also state-of-the-art results for X-band MMIC VCOs in GaN HEMT technology. The normalized phase noise at 1 MHz offset introduced in section 3.4 of the Ka-band GaN HEMT oscillator is also comparable with the state-of-the-art MMIC InGaP HBT-based oscillators for comparable frequency.

5.2 Low phase noise millimetre-wave signal source design in InP DHBT technology

This part presents the first architecture for realising low phase noise millimetre-wave sources in which the signal can be generated at fundamental millimetre-wave frequency, paper [E]. The designed oscillator is based on 130 nm InP DHBT process, see section 2.2, which is one of few transistor technologies available for fundamental millimetre-wave mode oscillator. The topology chosen is balanced Colpitts with schematic is presented in Fig. 5-1. A two-finger HBT with an emitter-finger length of 6 µm is selected, providing sufficient output power at specified oscillation frequency. Basically, the design is based on finding the optimal coupling between the active part and passive resonator. The whole passive resonator is EM-simulated for highest accurate simulation. Targeting high output power and low phase noise at 220 GHz, the design of the oscillator follows a special systematic method in which the complete resonator of a balanced Colpitts oscillator is represented with a black box model [72] and is defined in terms of four parameters: the resonant frequency (f_0), the resonator's impedance level (Z_c), the unloaded quality factor (Q_0), and the tapping ratio (n). These parameters can be converted to lumped-element component values representing the circuit in ADS. The design of the oscillator is an iterative process. Once, the four parameters of the resonator are parametrised to match with the EM simulated resonator, the optimisation is carried out on the schematic level for high output power and best possible phase noise at the specified oscillation frequency. Note that component values of the parametrised model are realistic numbers obtained in the actual technology, e.g. the Q factor must not be unrealistically high. After several iterations, the target performance is reached. In this design, the third metal layer MET3 is used as groundplane, see section 2.2. Except the lumped-component values of the resonator in the Colpitts' schematic, the bias network is also carefully designed. The output signal is extracted through a MIM capacitance of 10 fF at one side while the other port left open. The designed oscillator uses only one differential transistor pair without any additional combining networks, requiring less dc power consumption and therefore enabling higher power efficiency. The Computer-Aided-Design (CAD) layout and chip photo of the 220 GHz oscillator are shown in Fig. 5-9.

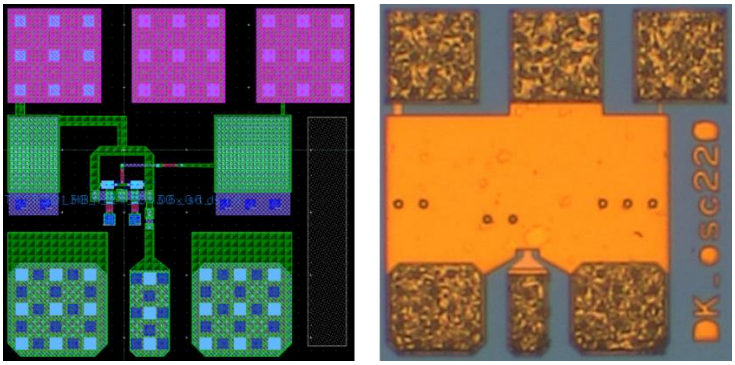


Fig. 5-9. CAD layout and chip photo of 220 GHz oscillator. Note that the goundplane MET3 is invisible in the CAD layout for a better view of the designed oscillator.

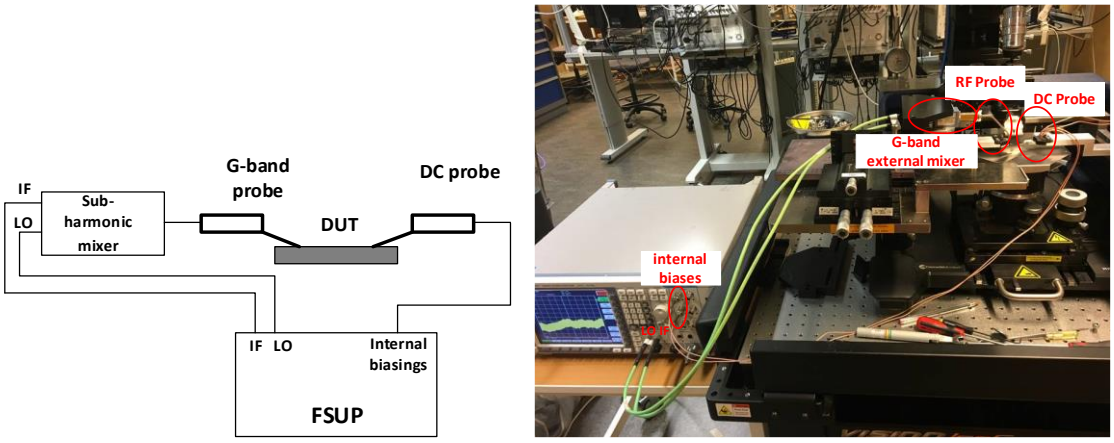
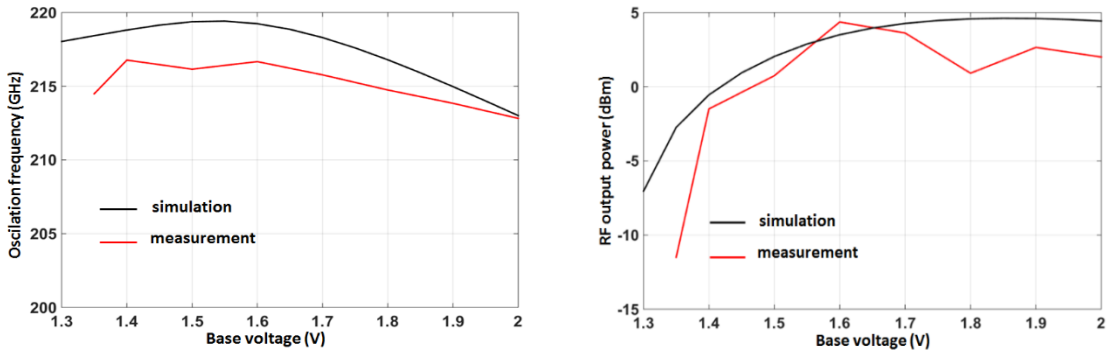


Fig. 5-10. Measurement setup.

The 220 GHz oscillator is characterised on-chip by the R&S FSUP50. The low noise internal dc supplies of the FSUP are used for biasing the base and the collector. The frequency range of the FSUP is extended using an external G-band sub harmonic mixer according to the measurement set-up in Fig. 5-10. The total loss from G-band probe and coaxial connection was characterised to be 2.5 dB.

Fig. 5-11 presents the simulated and measured oscillation frequency (a) and RF output power (b) of the designed 220 GHz oscillator versus base voltage at a collector voltage of 2 V. Both oscillation frequency and output power agree very well between measurements and simulations. The measured oscillation frequency varies from 213 to 217 GHz versus base voltage, which is down-shifted less than 2 % in comparison to the simulations. The peak output power is about 4.5 dBm in both measurements and simulations; however, there is a slight shift in the shape of measured and simulated output power. Moreover, the measured output power of 4.5 dBm is obtained for a relatively low collector current of 12 mA. It corresponds to a DC power consumption of 24 mW, translating into a dc-to-RF conversion efficiency > 10 %.



(a) (b)

Fig. 5-11. Measured results compared to ADS simulation. (a) Oscillation frequency. (b) Output power.

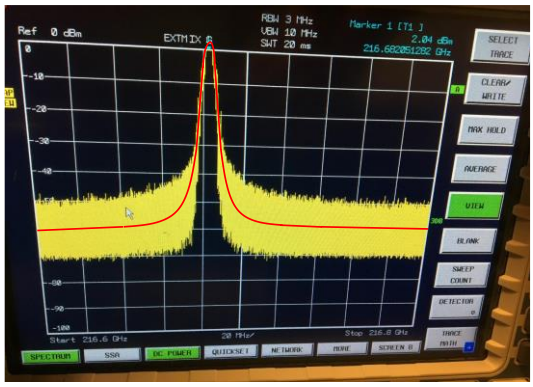
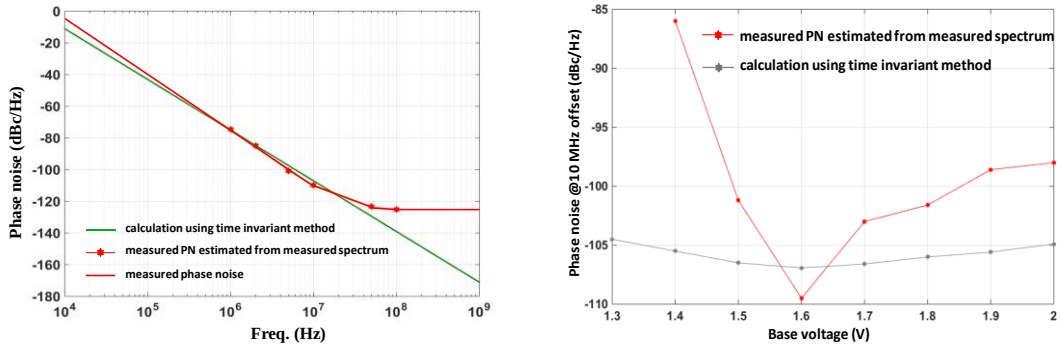


Fig. 5-12. Measured oscillator spectrum at bias condition, V_{cc} = 2 V, I_c = 12 mA.

The direct spectrum measurement presented in section 4.3.1 is used for phase noise characterisation of the presented oscillator. Fig. 5-12 shows measured oscillator spectrum for the peak output power bias condition, V_{cc} = 2 V, I_c = 12 mA. The measured phase noise at 10 MHz offset from Fig. 5-12 is calculated to

$$\mathcal{L}(10MHz) = -43 - 2 - 10\times\log_{10}(3\times10^{6}) \approx -110\ (dBc/Hz) \qquad (5\text{-}1)$$



(a) (b)

Fig. 5-13. Measured and calculated phase noise. (a) vesrus offset frequencies. (b) at 10 MHz offset versus bases voltage at V_{cc} = 2 V.

The same calculation may be repeated for other offset frequencies to present the phase noise slope versus offset frequency, see Fig. 5-13 (a). It can be noted that the phase noise spectrum of Fig. 5-13 (a) has a slope of -30 dB/decade inside f_m= 10 MHz while outside this frequency the slope appears to be -20 dB until the noise floor is reached at -125 dBc/Hz. The noise floor is caused by the measurement system, due to the FSUP's internal noise floor of -165 dBc/Hz and the harmonic mixers conversion loss of 40 dB [83]. In Fig. 5-13 (a), the calculated phase noise versus offset frequency based on the method in [68], is also shown. A good agreement is found at this minimum value of phase noise. However, measured phase noise and calculated phase noise at 10 MHz offset versus base voltage are somewhat different, as presented in Fig. 5-13 (b). A potential reason might be the large signal waveforms used for LTV calculation also include reactive currents from the device parasitics. The accuracy may be improved if the device model would be de-embedded for the intrinsic current.

TABLE 5-2
SUMMARY OF III-V TRANSISTOR BASED OSCILLATORS WITH OSCILLATION FREQUENCY>200GHZ

Ref.	Process	f_{osc} (GHz)	Peak P_{out} (dBm)	Min PN@10 MHz	P_{DC} (mW)	Peak dc-to-RF efficiency (%)	FOM* (dB)
[28]	0.13µm SiGe HBT	218-245	-3.6	-98	54	0.81	168
[29]	0.13µm SiGe HBT	212	-7.1	-92	30	0.65	164
[30]	0.13µm SiGe HBT	173-200	-3	-85	38	1.32	155
[31]	0.13µm SiGe HBT	237.2-249.8	-1.4	-87	15.5-26.5	1.95	162
[84]	0.25µm InP DHBT	305.8	5.3	-112**	87.4	3.88	183
[32]	0.25µm InP DHBT	247.8-262.2	2.9	-87.8	85	2.29	157
[33]	0.25µm InP DHBT	309.5-339.5	-6.5	-86.55	13.5	1.66	166
[34]	0.25µm InP DHBT	325	-5	-90.4	92.4	0.34	161
This work	**0.13µm InP DHBT**	**216.6**	**4.5±1.5**	**-110±3**	**24**	**11.74±3**	**183±3**

* *FOM* presented in section 3.4.
** Chose the highest value in the range given in [84].

Table 5-2 shows the comparison of the designed oscillator with state-of-the art III-V oscillators above 200 GHz reported in open literature. It is found that the designed oscillator has the highest conversion efficiency. In terms of output power and phase noise, the work in [84] has reported a bit higher output power and lower phase noise performance. However, the phase noise reported in [84] is likely an under-estimate since the curve is not smooth and a level shift on the order of 8 dB can be seen clearly from the phase noise spectrum. A realistic value is on the order of -110 dBc/Hz @10 MHz off-set, which is in line with the phase noise reported in this work. Translated to power normalized figure of merit (*FOM*) presented in section 3.4, the designed oscillator has *FOM* in excess of 180, which is matched only by the fixed-frequency oscillator reported in [84].

5.3 Low phase noise D-band signal source based on 0.15 µm GaN HEMT and 130 nm BiCMOS technologies

As already mentioned, millimetre-wave signal source can be also realised by the combination of intermediate high frequency oscillators and frequency multipliers. In paper [G], a D-band signal source based on this architecture is presented, see Fig. 5-14. A sufficient RF input power for the sixtupler is generated by the Ka-band GaN HEMT oscillator presented in section 5.1.2 operating at around 23 GHz. The particular motivation of using GaN HEMT oscillator is to reach the critical phase noise floor. The sixtupler is subsequently followed by a wideband 6-stage amplifier. They are implemented in 130 nm SiGe BiCMOS technology, presented in section 2.3. The amplifier is driven in compression to equalise the D-band output power, which is nearly independent of the oscillator's gate and drain voltages used for tuning the frequency of the source. Fig. 5-15 shows the chip photo of the presented D-band source in which the GaN oscillator is wire-bonded to the SiGe sixtupler and amplifier MMIC. This signal source not only has output RF probe for on-chip measurement, but also has an optional waveguide transition dedicated to bond-wire for future packaging as also seen in Fig. 5-15.

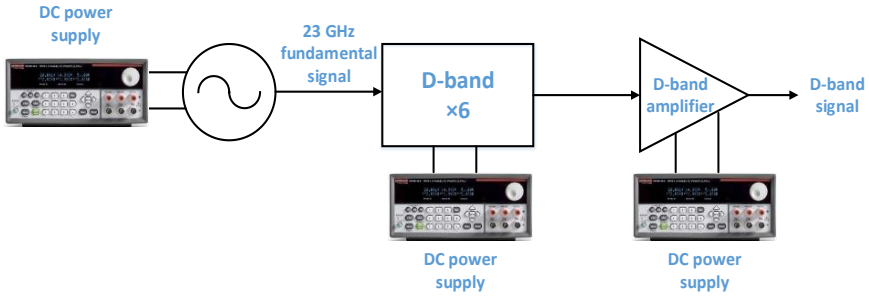


Fig. 5-14. Block diagram of the D-band signal source.

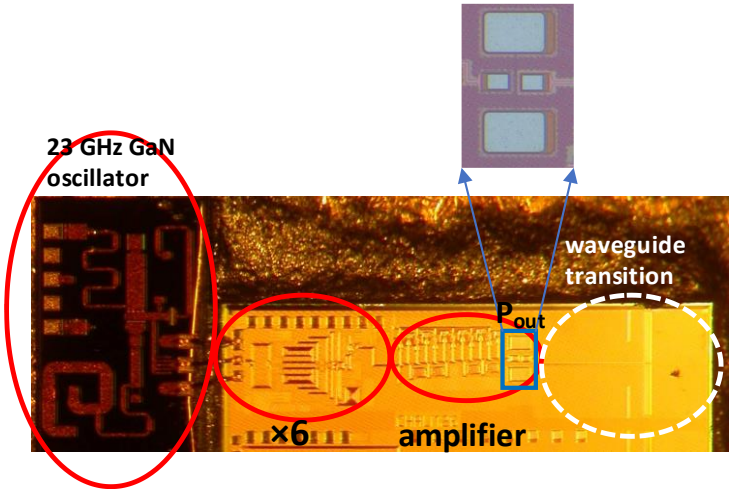


Fig. 5-15. Chip photo of the D-band signal source.

5.3.1 SiGe sixtupler and amplifier

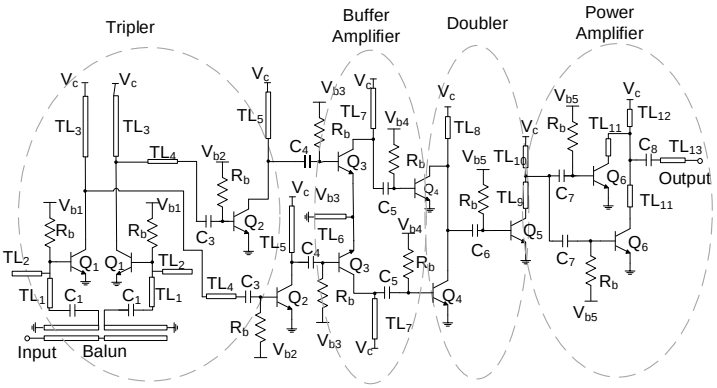


Fig. 5-16. Schematic of D-band SiGe sixtupler.

The schematic of the sixtupler, designed by M. Bao, is shown in Fig. 5-16, papers [F] and [G]. It consists of a balanced frequency tripler, followed by a buffer amplifier, a differential frequency doubler and a two-stage power amplifier. The single-ended input signal is converted into a differential signal by an on-chip balun. The inter-stage matching networks are designed between individual blocks, i.e. tripler, buffer amplifier, doubler, and power amplifier. In each design, harmonics up to the 6th order at output are simulated using harmonic balance algorithm. The transistors' size, biases, and the parameters of the passive components, i.e., capacitances, the length of the transmission line, etc., are chosen from the optimization with the targets of wide bandwidth, high output power and efficiency. The circuit is designed with Cadence. In order to reach highest accuracy in simulation, the transmission line and capacitor models from the design kit are replaced by EM models obtained from the Sonnet simulator. In this design, the metal layer 4 (M4) is used for the ground plane, see section 2.3. All transmission lines have a width of 5 µm with different lengths. The broad-side coupled transmission line in M6 and M5 are used to build a balun. Transistors Q_1 and Q_2 have two emitter fingers with a length of 6.3 µm each. The other transistors have a single emitter finger with a length of 10 µm.

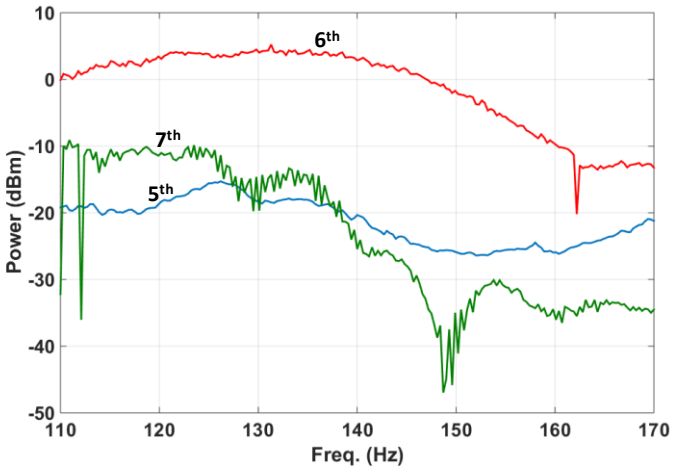


Fig. 5-17. Measured output power versus output frequency of the sixtupler

The sixtupler is characterised on-chip by a PNA-X Network Analyzer (N5247A) from Keysight. Millimetre-wave frequency extenders, i.e. WR-10 and WR-6.5 from Virginia Diodes, Inc., are used for W-band and D-band measurements, respectively. Two 4-channel programmable power supplies from Rohde & Schwarz HAMEG are used for DC bias.

Fig. 5-17 shows the power of the 5th, the 6th and the 7th harmonics of the sixtupler versus the output frequency (f_{out}), corresponding to the frequency of the input signal from 18.3 GHz to 28.3 GHz, i.e. $f_{out}/6$. The input power is fixed around 4.4 dBm. As shown in Fig. 5-17, the maximum output power is 4.5 dBm and the 3-dB bandwidth is 29 GHz (from 115 to 144 GHz). The rejection of the undesired 5th and 7th harmonics is larger than 10 dBc. The sixtupler consumes DC power of 310 mW and the maximum power efficiency is 0.9%. On top, the sixtupler exhibits a wide frequency bandwidth, a high output power in comparison with other frequency multipliers utilising SiGe BiCMOS technology [38, 85-87].

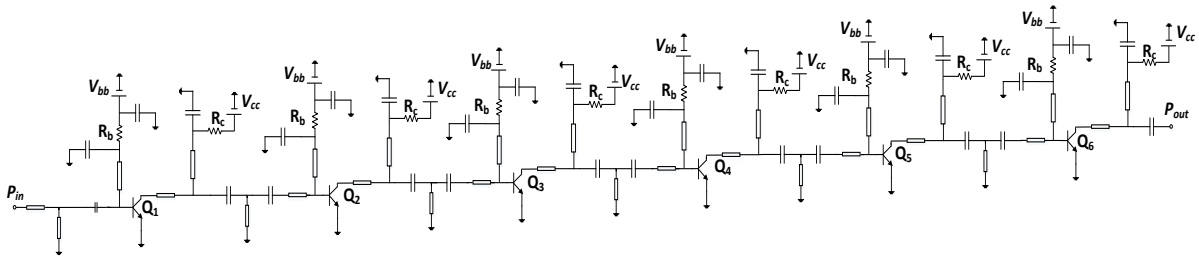
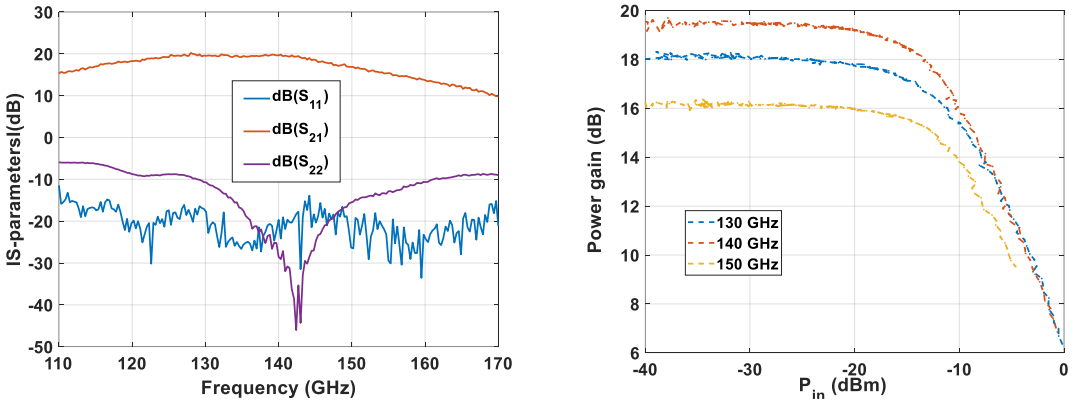


Fig. 5-18. Schematic of D-band SiGe amplifier.

Fig. 5-18 shows the schematic of the D-band amplifier, designed by H. Zirath, paper [G]. It consists of six cascaded stages common-emitter (CE) amplifier in order to achieve a sufficient amount of gain to get saturation for a given input. The matching networks are also designed to optimise the gain and the matching between stages. In order to achieve a large bandwidth, the lossy-matching concept employing the resistive loaded stub is used at each stage of the amplifier. All bases and collectors are biased through resistors of 200 Ω and 10 Ω, respectively. All transmission lines have width of 4.9 μm with different lengths and all transistors have emitter length of 4 μm.

The amplifier is also measured on-chip by a PNA-X Network Analyzer (N5247A) from Keysight and WR-6.5 extenders from Virginia Diodes, Inc. DC power supply from Rohde & Schwarz HAMEG is used for DC biasing.

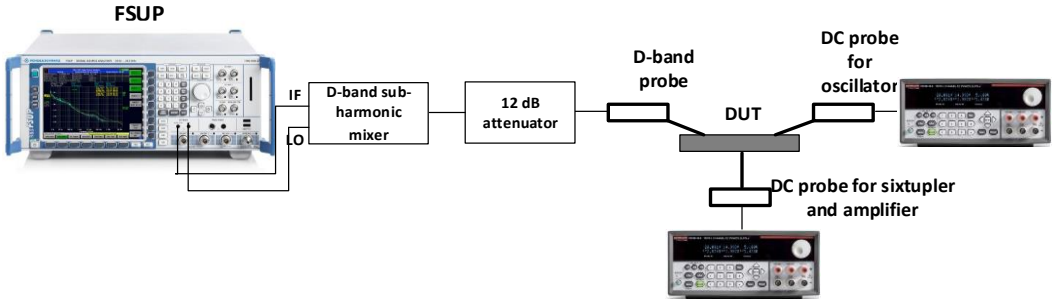
Fig. 5-19 (a) shows the measured small-signal S-parameters. A maximum small signal gain (S_{21}) of nearly 20 dB is obtained for the 6-stage amplifier and a 3-dB bandwidth is from 115 to 149 GHz. Over the whole D-band, the small signal gain is better than 10 dB and reflection coefficient at the input (S_{11}) and output (S_{22}) are lower than -6 and -10 dB, respectively. Fig. 5-19 (b) shows the measured power gain at 130 GHz, 140 GHz and 150 GHz, respectively when the input power is swept from -40 to 0 dBm. It can be seen that output gains get saturated at input power of -5 dBm for 130 and 140 GHz. The amplifier consumes DC power of 92 mW.



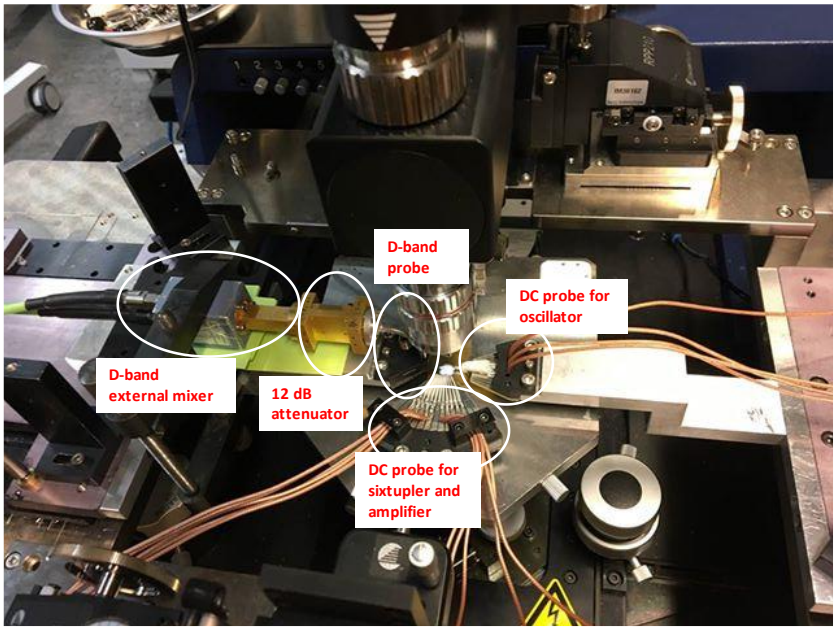
(a) (b)

Fig. 5-19. Measured power gain at 130 GHz, 140 GHz and 150 GHz, respectively when the input power is swept from -40 to 0 dBm.

5.3.2 Signal source performance



(a)

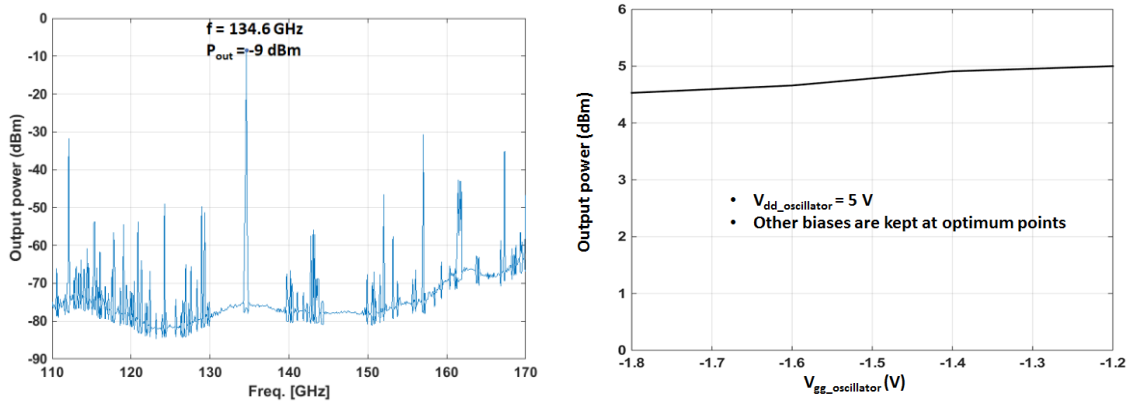


(b)

Fig. 5-20. Measurement setup. (a) Block diagram. (b) On-wafer test setup.

The D-band signal source is characterised on-wafer using the R&S FSUP50. The frequency range of the FSUP is extended using an external D-band sub harmonic mixer according to the measurement set-up in Fig. 5-20. A D-band fixed attenuator of 12 dB is also used in the setup, avoiding the power saturation due to the external mixer. The total loss from attenuator, D-band probe and coaxial connection was characterised to be 14 dB.

Fig. 5-21 (a) presents the measured output spectrum from R&S FSUP in the whole D-band. It is seen that D-band signals at around 135 GHz with output power about 5 dBm (after correction for probe and attenuator losses) are generated from the designed signal source. The harmonics suppression is better than 20 dB. Fig. 5-21 (b) presents output power of the designed signal source versus gate bias voltage of the GaN oscillator while drain bias voltage of the GaN oscillator (5 V) and other biases are fixed at optimum points. The output power of the signal source is almost constant at about 5 dBm over different oscillator's gate bias voltages, which is reasonable when considering the input-output power of the amplifier that is about 6 dBm, see Fig. 5-19 (b). It should be noted that the amplifier operates in compression mode to equalise the source output power so that it is nearly independent of the oscillator's gate and drain bias voltages used for tuning the source frequency. The small difference may be due to mismatch, losses in bondwires and sample-to-sample variations. A bandwidth of 1.3 GHz (from 134.5 to 135.8 GHz) is obtained by tuning the GaN oscillator's gate and drain bias voltages. The total DC power consumption of the signal source varies from 528 mW to 2.12 W over the tuning range.



(a) (b)

Fig. 5-21. Measured output spectrum. (a) from FSUP in D-band. (b) versus different gate bias voltages of the GaN oscillator (V_{dd_osc} = 5 V and other biases are fixed at the optimum points).

The measured phase noise at an off-set frequency of 10 MHz is estimated from the measured spectrum in Fig. 5-22 according to direct spectrum measurement methodology presented in section 4.3.1. It is about -128 dBc/Hz @ 10MHz offset frequency. However, it should be mentioned that this value is very near the measurement noise floor. The FSUP spectrum analyzer has a noise floor about -165 dBc/Hz which is degraded to about -130 dBc/Hz considering the conversion loss of the harmonic mixers (23 dB) and the 12 dB attenuation used.

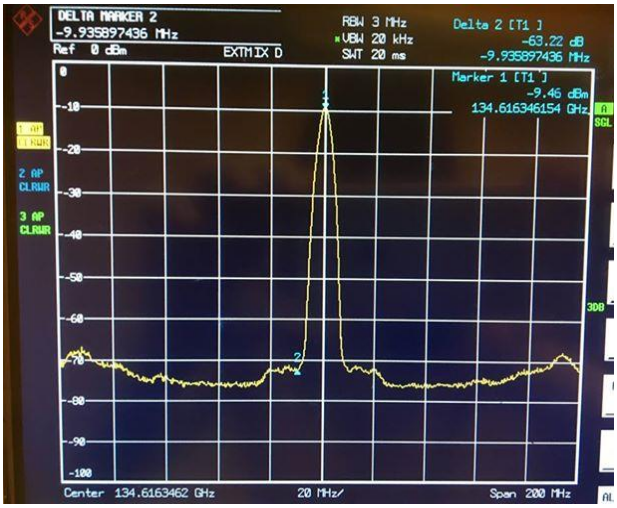


Fig. 5-22. Measured output spectrum from FSUP with frequency span of 200 MHz at V_{gg_osc} = -1.8 V, V_{dd_osc} = 5 V, other biases are fixed at optimum points.

Table 5-3 compares the performance of millimetre-wave signal sources in D-band using SiGe Bipolar and CMOS technologies reported in open literature. Each of them have different topologies as well as transistor technologies. It is seen that the presented signal source has high output power and the best phase noise. The normalized phase noise at 10 MHz offset of this signal source is a record number for a D-band signal source.

TABLE 5-3. SUMMARY OF SIGNAL SOURCES USING SIGE BIPOLAR AND CMOS TECHNOLOGIES IN D-BAND (110-170 GHZ)

Ref.	**Process/f_T/f_{max}**	**Architecture**	**f_o (GHz)**	**P_{out} (dBm)**	**BW (GHz)**	**PN @ 1MHz**	**PN @ 10 MHz**	**PN_{norm}@ 10MHz***
[88]	0.13µm SiGe BiCMOS/260/380	VCO + Tripler + Amp	160	5	7	-80**	-	-
[89]	0.13µm SiGe BiCMOS/-/135	Fundamental OSC	121	-3.5	0	-88	-102	183.6
[89]	0.13µm SiGe BiCMOS/-/135	Fundamental OSC	104	-2.7	0	-93.3	-105	185.3
[90]	Infineon's 0.35µm B7HF200/170/250	VCO + Doubler	144	3	39	-93	-	-
[91]	0.18 µm BiCMOS Technology	Osc + Amp + Doubler	133	3	0	-	-107.2	189.7
[92]	SiGe HBT/270/340	Push-push (second harmonic) osc + Amp	165	-3.5	0	-	-104**	188.3
[93]	SiGe HBT/300/450	Fundamental OSC	154	7	0	-87	-	-
[94]	SiGe/225/320	VCO + Amp	122	2	16	-95	-115	196.7
[95]	SiGe/170/250	VCO + Gilbert-Doubler	148	3	46	-94	-	
This work	**0.13µm BiCMOS /250/370 + 0.15µm AlGaN/GaN HEMT**	**Osc + Sixtupler + Amp**	**135**	**5**	**1.3**	**-112*** **	**-128 **** **	**210.6**

* Normalized phase noise presented in section 3.4

** Extrapolated using *20log(N)*

*** Estimated from residual phase noise at 10 MHz off-set

**** May be limited by noise floor of measurement system

Chapter 6

Conclusions

This thesis presents methods for design and analysis of MMIC low phase noise millimetre-wave signal source, targeted at wideband millimetre-wave communication applications. A couple of circuit demonstrators are included to exemplify the method used.

For the design of low phase noise oscillators, low frequency noise (LFN) is of particular interest due to the fact that it is up-converted to phase noise around the microwave signal. Thus, a benchmark of different III-V transistor technologies, e.g. GaN HEMTs, GaAs-InGaP HBTs, GaAs pHEMTs based on LFN performance is carried out. The experiments reveal that GaN HEMT is a good candidate for oscillators with strong requirements on far-carrier phase noise, e.g. wideband millimetre-wave wireless communications. This is verified by several state-of-the-art MMIC GaN HEMT based oscillators reported in this thesis, specifically X-band Colpitts VCOs and a Ka-band reflection type oscillator. The 1 MHz phase noise performance of the X-band GaN HEMT Colpitts VCOs and the Ka-band GaN HEMT reflection type oscillator are -135 and -129 dBc/Hz, respectively. Their phase noise performance at 1 MHz offset are state-of-the-art numbers for X-band MMIC VCOs and Ka-band MMIC oscillators, and even slightly better than state-of-the-art InGaP HBT based oscillators with comparable frequency and tuning range. Besides, measured phase noise in the $1/f^3$ region is well predicted with phase noise calculations applying the method in [68] based on Hajimiri's time invariant model and measured LFN data.

It has been seen that GaN HEMT based oscillators have better phase noise performance at far-carrier offsets, e.g. 1 MHz, but are often worse at near-carrier offsets, e.g. 100 kHz, compared to state-of-the-art InGaP HBT based oscillators. The main reason is the relatively high level of flicker noise in GaN HEMTs, resulting in a phase noise slope that is steeper than 30 dB/decade. Therefore, aiming for low phase noise oscillator design, methods to improve LFN characteristic of GaN HEMT devices such as different surface passivation and deposition methods and variations in transistor geometry are also investigated in this thesis. It is found that the LFN level of GaN based HEMTs can be lowered with well-selected passivation method, i.e. Al_2O_3 deposited with thermal ALD, leading to an improvement in oscillator phase noise. The effect of transistor geometry such as transistor size, gate length, gate width, etc., is insignificant.

Low phase noise millimetre-wave signal sources have been realised by two architectures in this work. In the first architecture, a MMIC G-band signal source designed at fundamental 220 GHz based on advanced 130nm InP DHBT technology is demonstrated. The designed oscillator targets high output power and low phase noise using a special design flow. The 220 GHz oscillator has measured output power of 5 dBm

and a phase noise at 10 MHz offset of -110 dBc/Hz, which are state-of-the-art values for an oscillator operating beyond 200 GHz. The dc to RF conversion efficiency of the 220 GHz oscillator is in excess of 10% which is the highest efficiency reported for a G-band MMIC oscillator in open literature. In the second architecture, a D-band signal source operating at 135 GHz is realised by the intermediate frequency Ka-band GaN HEMT oscillator demonstrated above and the state-of-the-art SiGe BiCMOS frequency sixtupler. The particular motivation of using the GaN HEMT oscillator is to reach low noise floor. The D-band signal source has a constant output power of 5 dBm and a record low phase noise for a D-band signal source, i.e. -128 dBc/Hz at 10 MHz offset. Translating to the frequency normalized phase noise at 10 MHz offset, shown in section 3.4, the first and second architectures have figures of merit of 197 and 210, respectively. It is clearly seen that the latter has better performance in this perspective. Further, the use of intermediate frequency for the VCO facilitates the frequency stabilization. To be used in a communication system, the VCO must be phase locked, e.g. with a PLL. Millimetre-wave PLLs are not yet commercially available and not easy to design. The future work includes demonstration of a frequency stabilised ultra-low noise floor millimetre-wave signal source based on an intermediate frequency GaN HEMT VCO followed by frequency multipliers and connected to integrated frequency dividers enabling phase locking with a commercial PLL.

Summary of Appended Papers

Paper [A]

Low Frequency Noise Measurements - A Technology Benchmark with Target on Oscillator Applications

In this paper, the low frequency noise measurements and benchmark parameters of commercial devices in different III-V transistor technologies such as GaN HEMTs, InGaP HBTs, GaAs pHEMTs presented for low phase noise oscillator design are presented.

My contribution is low frequency noise characterisations, analysis of the results and writing the paper.

Paper [B]

Effects of Surface Passivation and Deposition Methods on the *1/f* Noise Performance of AlInN/AlN/GaN High Electron Mobility Transistors

In this paper, the effects of surface passivation and deposition methods on the *1/f* noise performance of AlInN/AlN/GaN HEMT devices are analysed. The devices are fabricated by Anna Malmros.

My contribution is low frequency noise characterisations, analysis of the results and writing the paper.

Paper [C]

A MMIC GaN HEMT Voltage-Controlled-Oscillator with High Tuning Linearity and Low Phase Noise

This paper reports a MMIC GaN HEMT based VCO with state-of-the-art performance. The design is also combined with phase noise calculation based on time-invariant method.

My contribution is designing the oscillator, characterisation, analysis of the results and writing the paper.

Paper [D]

7-13 GHz MMIC GaN HEMT Voltage-Controlled-Oscillators (VCOs) for satellite applications

In this paper, a X-band VCO chip set implemented in GaN HEMT technology covering the frequency from 7-13 GHz for satellite applications is presented. The design is also combined with phase noise calculation based on time-invariant method.

My contribution is designing the oscillator, characterisation, analysis of the results and writing the paper.

Paper [E]
220 GHz Oscillator in 130 nm InP HBT MMIC Technology

This paper reports a fundamental 220 GHz signal source implemented in advanced 130 nm InP DHBT technology with state-of-the-art performance. The oscillator was originally designed by D. Kuylenstierna, and then re-simulated by me. The design is also combined with phase noise calculation based on time-invariant method.

My contribution is characterisation, phase noise calculation, analysis of the results and writing the paper.

Paper [F]
A 110-147 GHz Frequency Sixtupler in a 130 nm SiGe BiCMOS Technology

This paper presents a state-of-the-art frequency sixtupler in a 130 nm SiGe BiCMOS technology.

The circuit is designed by Mingquan Bao. My contribution is characterisation of circuit.

Paper [G]
A low phase noise D-band signal source based on 130 nm SiGe BiCMOS and 0.15 µm AlGaN/GaN HEMT Technologies

In this work, a low phase noise D-band signal source is realised by the low phase noise Ka-band GaN HEMT oscillator and state-of-the-art MMIC SiGe BiCMOS of a sixtupler and an amplifier. This is the paper invited to extend the work in paper [F] for special issue on EuMW 2018. The oscillator is originally designed by D. Kuylenstierna, the sixtupler and the amplifier were originally designed by M. Bao and H. Zirath, respectively.

My contribution is assembly, characterisation, analysis of the results and writing the paper.

Acknowledgement

The journey towards my PhD degree has been fulfilled with both challenges and joyfulness. Now as that journey finally comes to the end, I would like to express my gratitude to the people who have been supporting me during my PhD study.

First, I would like to express my gratitude to my examiner, Prof. Herbert Zirath for having given me the opportunity to work in the Microwave Electronics Laboratory and to join in his numerous projects that I have gained a great deal of circuit design experience with different transistor technologies. I'm also grateful to him for the time he had put into reviewing the manuscripts and thesis.

My sincere and deep gratitude goes to my main supervisor, Assoc. Prof. Dan Kuylenstierna for his inspired guidance, insightful advice, careful review, valuable suggestions, great patience and constant encouragement and support throughout the entire period of my research study. In short, thanks for being a great supervisor.

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